DYNAMIC RAM MODULES DATA BOOK

FALL 1995

NEC

DATA BOOK Fall 1995



Dynamic

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Modules

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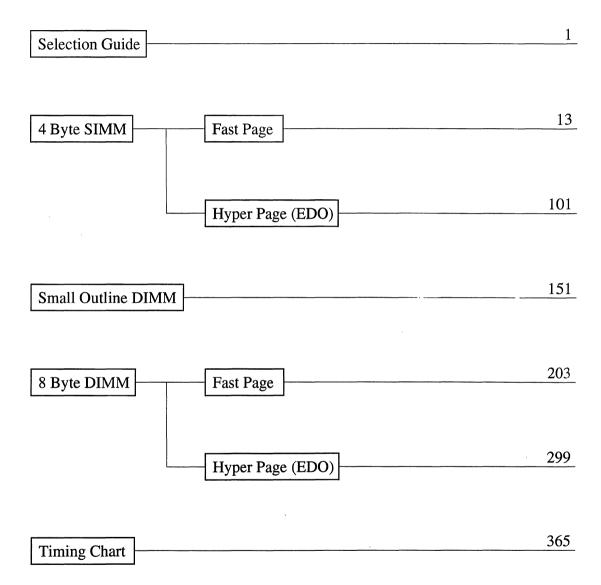


Dynamic RAM Module Fall 1995 Data Book

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-NOTES FOR CMOS DEVICES -

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to Vod or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

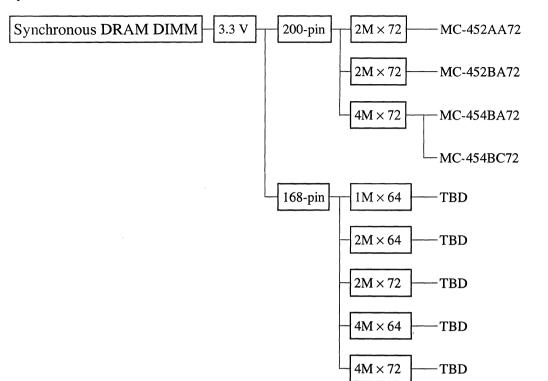
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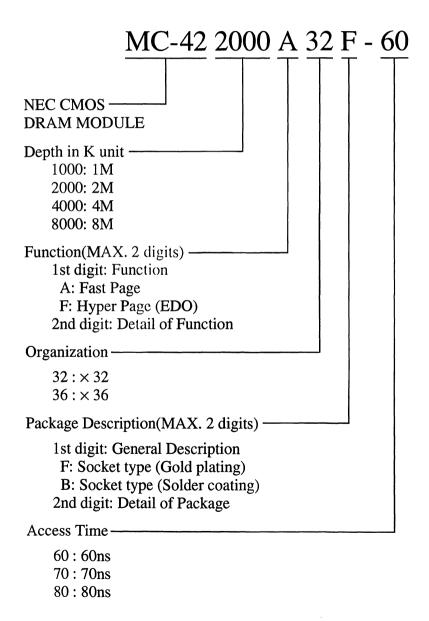
Synchronous DRAM DIMM.....TBD



Selection Guide

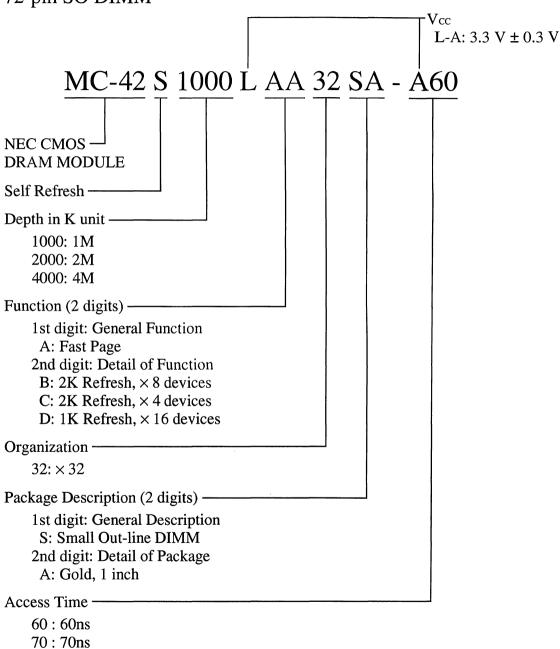
Part Number

72-pin SIMM



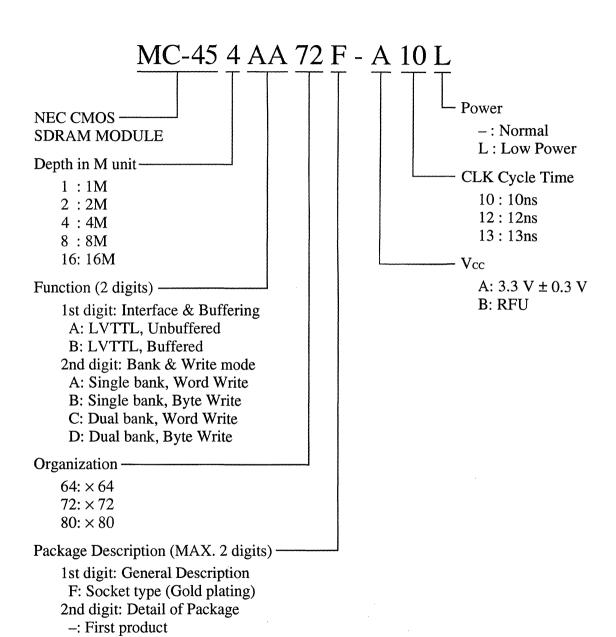
72-pin SO DIMM

80:80ns



 $: 5.0 \text{ V} \pm 0.25 \text{ V}$ L-A: $3.3 \text{ V} \pm 0.3 \text{ V}$ MC-42 S 4000 L AB 72 F - A60 NEC CMOS DRAM MODULE Self Refresh -Depth in K unit -1000: 1M 2000: 2M 4000: 4M Function (2 digits) -1st digit: General Function A: Fast Page F: Hyper Page (EDO) 2nd digit: Detail of Function A: 1K Refresh, Parity or Non parity B: 2K Refresh, ECC C: 4K Refresh, ECC D: 1K Refresh, ECC Organization · $64: \times 64$ $72: \times 72$ Package Description (MAX. 2 digits) 1st digit: General Description F: Socket type (Gold plating) 2nd digit: Detail of Package -: TSOP, linch (First product) Alphabetical order in the same configuration and function Access Time 60:60ns 70:70ns 80:80ns

200-pin 8 Byte SDRAM DIMM



72-pin SIMM Fast Page Line-up (× 32)

		Access Time	Refresh	Supply		Package			Monolithic Device)	Domanic
Organization	Part Number	(ns)	Cycle	Voltage	Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	Remark
	MC-421000A32B	60, 70, 80,			Single	S/C		11.4 4	1.00 0.00	8	
11422	MC-421000A32F	100			side	G/P		1M×4	300 mil SOJ	8	
1M×32	MC-421000A32BA	CO 70 CO			Single	S/C		11.410	400 1 60 1		
	MC-421000A32FA	60, 70, 80	4 1/40	,	side	G/P		1M×16	400 mil SOJ	2	
	MC-422000A32B	60, 70, 80	1 K/16 ms			S/C		44.4	200 3 50 1	16	
01400	MC-422000A32F	100		5.0	side	G/P	4	1M×4	300 mil SOJ	16	
2M × 32	MC-422000A32BA	CO 70 00		5.0 ± 0.5 V	Double	S/C	1 inch	11416	400: 1 60 1	4	
	MC-422000A32FA	60, 70, 80			side	G/P		1M×16	400 mil SOJ	4	
41.4.4.22	MC-424000A32B	60 70 00			Single	S/C		454 4	200 1 50 1		
4M×32	MC-424000A32F	60, 70, 80	2 K/32 ms		side	G/P		4M × 4	300 mil SOJ	8	
8M×32	MC-428000A32B	60.70.00	2.402 1110		Double	S/C		4544	200 100 1	10	
61VI X 32	MC-428000A32F	60, 70, 80			side	G/P		4M × 4	300 mil SOJ	16	

S/C: Solder Coated, G/P: Gold Plated

72-pin SIMM Fast Page Line-up (× 36)

		Access Time	Refresh	Supply		Package			Monolithic Device		
Organization	Part Number	(ns)	Cycle	Voltage	Mounted side	Edge connector	Height (inch)	Org.	Pkg.	Amt.	Remark
	MC-421000A36BJ		70, 80, 100		Single	S/C	1.05	1M × 4	300 mil SOJ	8	
1M × 36	MC-421000A36FJ	70, 80, 100			side	G/P	1.25	1M × 1	300 mil SOJ	4	
	MC-421000A36BE		41/40		Double	S/C		1M × 4	300 mil SOJ	8	
	MC-421000A36FE		1K/16 ms		side	G/P	1.0	1M × 1	300 mil SOJ	4	
-											
2M × 36	MC-422000A36BJ	70, 80, 100		5.0 ± 0.5 V	Double	S/C		1M × 4	300 mil SOJ	16	
	MC-422000A36FJ				side	G/P	1.25	1M × 1	300 mil SOJ	8	
	MC-424000A36BJ				Single	S/C	1.05	4M × 4	300 mil SOJ	8	
43.4	MC-424000A36FJ	00 70 00			side	G/P	1.25	4M × 1	300 mil SOJ	4	
4M × 36	MC-424000A36BE	60, 70, 80	01//00		Double	S/C	1.0	4M × 4	300mil SOJ	8	
	MC-424000A36FE		2N32 MS	2K/32 ms	side	G/P	1.0	4M × 1	300mil SOJ	4	
8M×36	MC-428000A36BJ	60, 70, 80			Double	S/C	1.05	4M × 4	300 mil SOJ	16	
OIVI X 30	MC-428000A36FJ	60, 70, 80			side	G/P	1.25	4M × 1	300 mil SOJ	8	

S/C: Solder Coated, G/P: Gold Plated

72-pin SIMM Hyper Page (EDO) Line-up

		Access Time	Refresh	Refresh Supply		Package		Monolithic Device			Damark
Organization	Part Number	(ns)	Cycle	Voltage	Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	Remark
11422	MC-421000F32BA	60.70			Single	S/C		1M×16	400 mil SOJ		
1M×32	MC-421000F32FA	60, 70	1 4 1/10	side	G/P		TIVIXIO	400 11111 303	2		
20.422	MC-422000F32BA	1 K/16 ms		Double	S/C		1M×16	400 mil SOJ	4		
2M × 32	MC-422000F32FA	60, 70		5.0 ±	side	G/P	4	I IVI X IO	400 mii 503	4	
41.422	MC-424000A32B	00.70		0.5 ∵	Single	S/C	1 inch	45.4	200 - 3 50 1		
4M×32	MC-424000A32F	60, 70	0.1/100		side	G/P		4M × 4	300 mil SOJ	8	
8M×32	MC-428000A32B	60.70	2 K/32 ms		Double	S/C		45.44			
81VI X 32	MC-428000A32F	60, 70			side	G/P		4M × 4	300 mil SOJ	16	

S/C: Solder Coated, G/P: Gold Plated

72-pin Small Outline DIMM Line-up

0	Part Number	Access Time	Supply	Refresh	Refresh Bank		Mor	nolithic Device		D
Organization	Part Number	(ns)	Voltage	Cycle	org.	Package	Org.	Pkg.	Amt.	Remark
1M×32	MC-42S1000LAD32SA	60, 70, 80		1 K/128 ms	1		1M × 16	400 mil TSOP	2	
21422	MC-42S2000LAB32SA	60, 70, 80		2 K/128 ms	1		2M × 8	400 mil TSOP	4	
2M × 32	MC-42S2000LAD32SA	60, 70, 80	3.3 ± 0.3 V	1 K/128 ms	2	72-pin SOD Gold plated	1M×16	400 mil TSOP	4	
454	MC-42S4000LAB32SA	60, 70, 80		2 V/120	2		2M×8	400 mil TSOP	8	
4M × 32	MC-42S4000LAC32SA	60, 70, 80		2 K/128 ms	1		4M × 4	300 mil TSOP	8	

168-pin 8 Byte DIMM Fast Page Line-up

	5	Access Time	Refresh	Supply	Packa	ige	Λ	Ionolithic Device		- Remark
Organization	Part Number	(ns)	Сус'е	Voltage	Edge connector	Height	Org.	Pkg.	Amt.	nemark
414 . 64	MC-421000AA64FA	60, 70, 80			i		1M×4	300 mil SOJ	16	
1M×64	MC-421000AA64FB	60, 70, 80	1 K/40				1M × 16	400 mil SOJ	4	
2M × 64	MC-422000AA64FB	60, 70, 80	1 K/16 ms	5.0 ±			1M×16	400 mil SOJ	8	
1M × 72 ECC	MC-421000AD72F	60, 70, 80		0.25 V			1M × 16 1M × 4	400 mil TSOP 300 mil TSOP	4 2	
2M × 72	MC-422000AB72F	60, 70, 80			Gold plated	1 inch	2M × 8	400 mil TSOP	9	
ECC	MC-422000LAB72F	60, 70, 80	0.14/00	3.3 ± 0.3 V			2M×8	400 mil TSOP	9	
	MC-424000AB72F	60, 70, 80	2 K/32 ms	5.0 ± 0.25 V			4M × 4	300 mil TSOP	18	
4M × 72 ECC	MC-424000LAB72F	60, 70, 80		3.3 ± 0.3 V			4M × 4	300 mil TSOP	18	
	MC-424000AC72F	60, 70, 80	4 K/64 ms	5.0 ± 0.25 V			4M × 4	300 mil TSOP	18	

168-pin 8 Byte DIMM Hyper Page (EDO) Line-up

		Access Time	Refresh	Refresh Supply Package					Monolithic Device)	Bonnelle
Organization	Part Number	(ns)	Cycle	Voltage	Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	Remark
1M × 64	MC-421000FA64FB	60, 70	1 K/16 ms		Single side			1M×16	400 mil SOJ	2	
2M × 64	MC-422000FA64FB	60, 70	INTOMS	5.0 ± 0.5 V	Double side			1M × 16	400 mil SOJ	4	
01470	MC-422000FB72F	60.70	2 K/22		Double	Cold plated	1 inch	2M×8	400 mil TSOP	0	
2M × 72	MC-422000LFB72F	60, 70	2 K/32 ms	3.3 ± 0.3 V	side	Gold plated	1 inch	2 2 1 VI X 8	400 mii 150P	9	
414 ~ 70	MC-424000FC72F	60.70	4 V/64 ma	5.0 ± 0.5 V	Double			4M × 4	300 mil TSOP	18	
4M × 72	MC-424000LFC72F	60, 70	4 K/64 ms	3.3 ± 0.3 V	side			41VI X 4	300 11111 130P		

٦

200-pin SDRAM DIMM Line-up

		5	Bank	Min.Cycle	Supply	Pac	kage	Monolith	nic Device	Describ
	Organization	Part Number	Org.	time (ns)	Voltage	Edge connector	Height	Org.	Amt.	Remark
11-1-4	2M × 72	MC-452AA72F	Single				20.2 mm	2M × 8	9	TBD
Unbuffered							29.2 mm			
	2M × 72	MC-452BA72F	Single	1 10 (100 MHz)				2M × 8	9	TBD
				12 (83 MHz)	3.3 ±	Gold				
Buffered	4M×72	MC-454BA72F	Single	13 (77 MHz)	0.3 V	plated	20.1	4M × 4	18	TBD
Bullered	4IVI X 72	MC-454BC72F	Dual				38.1 mm	2M × 8	18	TBD

4 Byte SIMM [Fast Page]

DATA SHEET



MOS INTEGRATED CIRCUIT MC-421000A32BA, 421000A32FA

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32BA, 421000A32FA are 1,048,576 words by 32 bits dynamic RAM module on which 2 pieces of 16 M DRAM: μ PD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- · 1,048,576 words by 32 bits organization
- · Fast access and cycle time

Family	Family Access time R/W cycle time		1	onsumption //AX.)
(MAX.) (MIN.)	(MIN.)	Active	Standby	
MC-421000A32-60	60 ns	110 ns	1,760 mW	11 mW
MC-421000A32-70	70 ns	130 ns	1,650 mW	(CMOS level input)
MC-421000A32-80	80 ns	150 ns	1,540 mW	

- 1,024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.



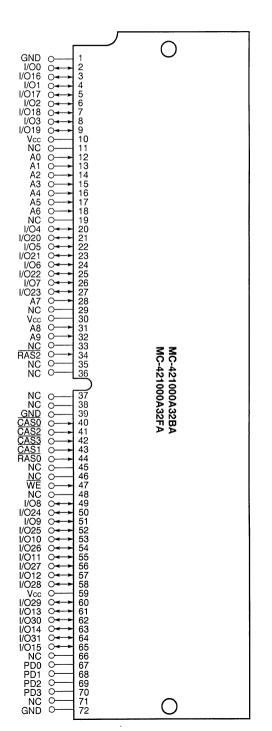
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32BA-60	60 ns	72-pin Single In-line Memory Module	2 pieces of μPD4218160LE
MC-421000A32BA-70	70 ns	(Socket Type)	(400 mil SOJ)
MC-421000A32BA-80	80 ns	Edge connector: Solder coating (HAL)	[Single side]
MC-421000A32FA-60	60 ns	72-pin Single In-line Memory Module	[
MC-421000A32FA-70	70 ns	(Socket Type)	
MC-421000A32FA-80	80 ns	Edge connector: Gold plating	



Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0 - A9 : Address Inputs

I/O0 - I/O31 : Data Inputs/Outputs

CASO - CAS3 : Column Address Strobe

RASO, RAS2 : Row Address Strobe

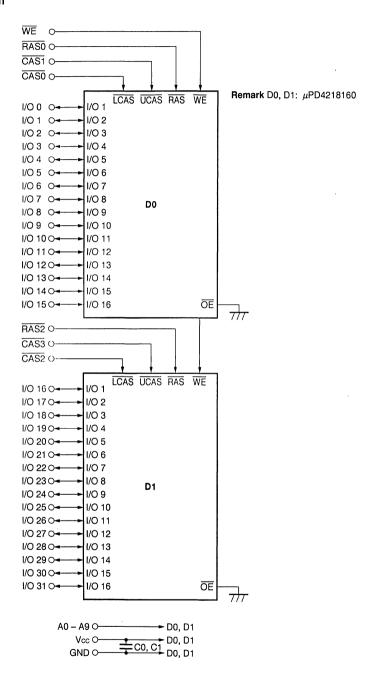
WE : Write Enable
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	Pin Access Time			
Name	No.	60 ns	70 ns	80 ns	
PD0	67	GND	GND	GND	
PD1	68	GND	GND	GND	
PD2	69	NC	GND	NC	
PD3	70	NC	NC	GND	



Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Po		2	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.5	5.0	5.5	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance ($T_A = 25$ °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A9			30	
	C ₁₂	WE			34	_
	Сіз	RASO, RAS2			22	pF
	C14	CASO - CAS3			22	
Data Input/Output capacitance	C _{I/O}	I/O0 - I/O31			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling	trac = 60 ns		320		
		Inc = URC (MIN.) Io = 0 mA	trac = 70 ns		300	mA	3, 4, 7
		10 - 0 111/1	trac = 80 ns		280		
Standby current	lcc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		4	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		2		
RAS only refresh current	lccs	RAS Cycling	trac = 60 ns		320		
		TAS ≥ Vih (MIN.) trc = trc (MIN.)	trac = 70 ns		300	mA	3, 4, 5, 7
		lo = 0 mA	trac = 80 ns		280		ļ
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		180		
(Fast page mode)	ľ	tpc = tpc (MIN.) Io = 0 mA	trac = 70 ns		160	mA	3, 4, 6
		IO = U IIIA	trac = 80 ns		140		
CAS before RAS	lcc5	RAS Cycling	trac = 60 ns		320		
refresh current		trc = trc (MIN.)	trac = 70 ns		300	mA	3, 4
		10 = U MA	trac = 80 ns		280		
Input leakage current	lı (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10	+10	μΑ	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μΑ	
High level output voltage	Vон	lo = -2.5 mA		2.4		٧	
Low level output voltage	Vol	lo = +2.1 mA			0.4	٧	



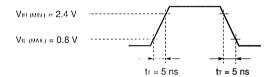
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

_		trac	= 60 ns	trac	= 70 ns	trac	= 80 ns	Ī	Γ
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	tric	110		130		150		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	toac		15		20		20	ns	10, 11
Access Time Column Address	tan		30		35		40	ns	10, 11
Access Time from CAS Precharge	tace		35		40		45	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcız	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	tre	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tяsн	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	5		5		5		ns	
RAS Hold Time from CAS Precharge	trhcp	35		40		45		ns	
Row Address Setup Time	tasr	0		0		0		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	t CAH	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	tarh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twcн	10		10		15		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr.	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	tref		16		16		16	ms	

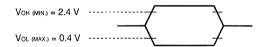


Notes

- 1. All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight CAS before RAS or RAS only refresh
 cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- loc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc₁ and Icc₃ are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.)
 and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition
 - (1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and tred ≤ tred (MAX.)	trac (MAX.)	trac (MAX.)
trad > trad (MAX.) and tred ≤ tred (MAX.)	taa (MAX.)	trad + taa (max.)
trod > trod (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or tax) is to be used for finding out when output data will be available. Therefore, the input conditions $trad \ge trad (MAX.)$ and $trad \ge trad (MAX.)$ will not cause any operation problems.

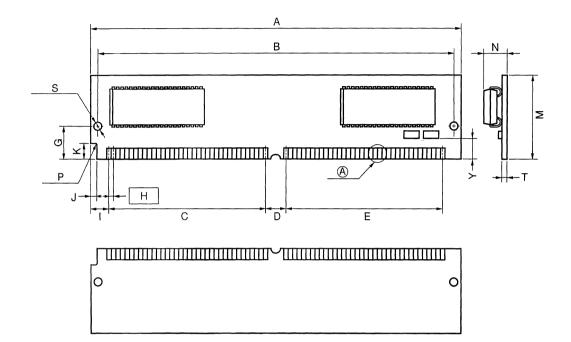
- 11. Loading conditions are 1 TTL and 100 pF.
- toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trich (MIN.) or trich (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the \overline{CAS} falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

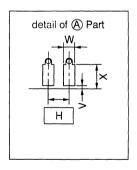
Timing Chart

Please refer to Timing Chart 1, page 365.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
Р	R1.57	R0.062
S	φ3.18	φ0.125
Т	1.27 ^{+0.1} _{-0.08}	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Υ	3.17 MIN.	0.124 MIN.

M72B-50A46

DATA SHEET



MOS INTEGRATED CIRCUIT MC-421000A32, 421000A36 SERIES

1 M-WORD BY 32-BIT, 1 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32 series is a 1,048,576 words by 32 bits dynamic RAM module on which 8 pieces of 4 M DRAM: µPD424400 are assembled.

The MC-421000A36 series is a 1,048,576 words by 36 bits dynamic RAM module on which 8 pieces of 4 M DRAM: μ PD424400 and 4 pieces of 1 M DRAM: μ PD421000 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 32 bits organization (MC-421000A32 series)
- 1,048,576 words by 36 bits organization (MC-421000A36 series)
- · Fast access and cycle time

Family	Access time	R/W cycle time (MIN.)	Power consumption (MAX.)		
	(IVIAX.)	(IVIIIV.)	Active	Standby	
MC-421000A32-60	60 ns	120 ns	5,280 mW		
MC-421000A32-70	70 ns	140 ns	4,400 mW	44 mW	
MC-421000A32-80	80 ns	160 ns	3,960 mW	(CMOS level input)	
MC-421000A32-10	100 ns	190 ns	3,520 mW		
MC-421000A36-70	70 ns	140 ns	6,160 mW	66 mW	
MC-421000A36-80	80 ns	160 ns	5,500 mW	(CMOS level input)	
MC-421000A36-10	100 ns	190 ns	4,840 mW		

- · 1,024 refresh cycles/16 ms
- · CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.



Ordering Information

[MC-421000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32B-60	60 ns	72-pin Single In-line Memory Module	8 pieces of μPD424400LA
MC-421000A32B-70	70 ns	(Socket Type) Edge connector: Solder coating (HAL)	(300 mil SOJ)
MC-421000A32B-80	80 ns	Edge connector. Solder coating (HAL)	[Single side]
MC-421000A32B-10	100 ns		(emgio orde)
MC-421000A32F-60	60 ns	72-pin Single In-line Memory Module	
MC-421000A32F-70	70 ns	(Socket Type) Edge connector: Gold plating	
MC-421000A32F-80	80 ns	Lage connector. Gold planning	
MC-421000A32F-10	100 ns		

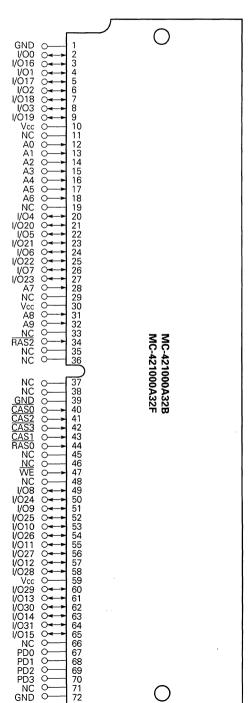
[MC-421000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices	
		72-pin Single In-line Memory Module	8 pieces of μPD424400LA	
MC-421000A36BE-70	70 ns	(Socket Type)	(300 mil SOJ)	
MC-421000A36BE-80	80 ns	Edge connector: Solder coating (HAL)	4 pieces of μPD421000LA	
MC-421000A36BE-10	100 ns		(300 mil SOJ)	
		72-pin Single In-line Memory Module	7	
MC-421000A36FE-70	70 ns	(Socket Type)	[Double side]	
MC-421000A36FE-80	80 ns	Edge connector: Gold plating		
MC-421000A36FE-10	100 ns			
		72-pin Single In-line Memory Module	8 pieces of μPD424400LA	
MC-421000A36BJ-70	70 ns	(Socket Type)	(300 mil SOJ)	
MC-421000A36BJ-80	80 ns	Edge connector: Solder coating (HAL)	4 pieces of μPD421000LA	
MC-421000A36BJ-10	100 ns		(300 mil SOJ)	
		72-pin Single In-line Memory Module		
MC-421000A36FJ-70	70 ns	(Socket Type)	[Single side]	
MC-421000A36FJ-80	80 ns	Edge connector: Gold plating		
MC-421000A36FJ-10	100 ns			

Pin Configuration

[MC-421000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0 - A9 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs

CASO - CAS3 : Column Address Strobe

RAS0, RAS2 : Row Address Strobe

WE : Write Enable
Vcc : Power Supply
GND : Ground
NC : No connection

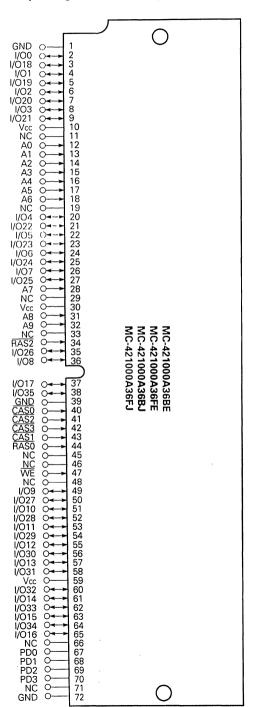
The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND



[MC-421000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0 - A9 : Address Inputs

I/O0 - I/O35 : Data Inputs/Outputs

CASO - CAS3 : Column Address Strobe

RAS0, RAS2 : Row Address Strobe

WE : Write Enable
Vcc : Power Supply
GND : Ground

NC : No connection

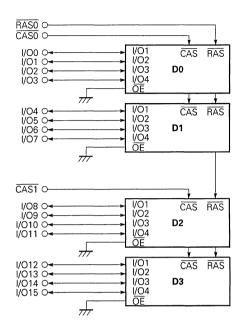
The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin		Access	Time	
Name	No.		70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

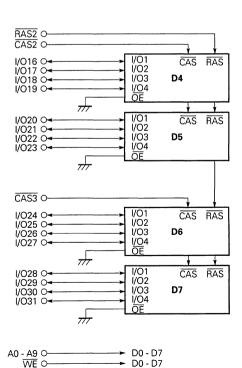


Block Diagram

[MC-421000A32 series]



Remark D0 - D7 : μPD424400



D0 - D7

D0 - D7

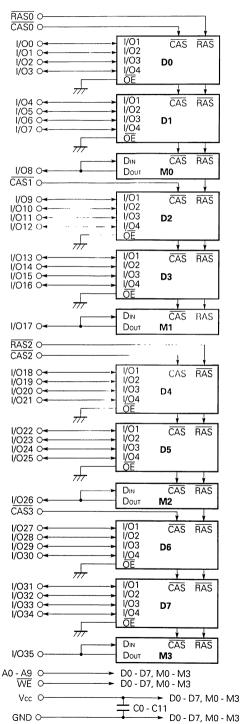
C0 - C7

Vcc ○

GND O-

NEC

[MC-421000A36 series]



Remark D0 - D7 : μ PD424400 M0 - M3 : μ PD421000



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Ро	MC-421000A32	8	
·		MC-421000A36	12	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tato		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.5	5.0	5.5	٧
High level input voltage	Vih		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz) [MC-421000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A9			68	
	Cı2	WE			76	
	Сіз	RASO, RAS2			43	pF
	Cia	CASO - CAS3			29	
Data Input/Output capacitance	Ci/o	I/O0 - I/O31			17	pF

[MC-421000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A9			88	
	Cı2	WE			104	_
	Сіз	RASO, RAS2			57	pF
	C ₁₄	CASO - CAS3			36	
Data Input/Output capacitance	Ci/O1	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	C1/O2	1/08, 1/017, 1/026, 1/035			22	



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-421000A32 series]

Parameter	Symbol	Test condition	1	MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling trc = trc (MIN.)	trac = 60 ns		960 800		
		lo = 0 mA	trac = 70 ns		720	mA	3, 4, 7
			trac = 100 ns		640		
O. II '							-
Standbý current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		16	mA	
		RAS, CAS ≥ Vcc – 0.2 V	lo = 0 mA		8		
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		960		
		CAS ≥ Vih (MIN.)	trac = 70 ns		800	mA	3, 4, 5, 7
		lo = 0 mA	trac = 80 ns		720	1777	0, 4, 0, 7
			trac = 100 ns		640		
Operating current	Icc4	RAS & VIL (MAX.), CAS Cycling	trac = 60 ns		720		
(Fast page mode)			trac = 70 ns		640	mA	3, 4, 6
		lo = 0 mA	trac = 80 ns		560		3, 4, 0
			trac = 100 ns		480		
CAS before RAS	lcc5	RAS Cycling	trac = 60 ns		960		
refresh current		trc = trc (MIN.)	trac = 70 ns		800	mA	3, 4
		10 = 0 MA	trac = 80 ns		720	11114	3, 4
			trac = 100 ns		640		
Input leakage current	li (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10	+10	μΑ	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μΑ	
High level output voltage	Vон	lo = -5.0 mA		2.4		V	
Low level output voltage	Vol	lo = +4.2 mA			0.4	٧	



[MC-421000A36 series]

Parameter	Symbol	Test condition	1	MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling					
		trc = trc (MIN.)	trac = 70 ns		1,120	mA	3, 4, 7
		10 - 0 1112	trac = 80 ns		1,000	111/2	3, 4, 7
			trac = 100 ns		880		
Standby current	Icc2	RAS, CAS ≥ VIH (MIN.)	lo = 0 mA		24	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		12	l IIIA	
RAS only refresh current	Іссз	RAS Cycling					
		CAS ≥ Vih (MIN.) trc = trc (MIN.)	trac = 70 ns		1,120	m 1	2 4 5 7
	TRC = T Io = 0		trac = 80 ns		1,000		3, 4, 5, 7
			trac = 100 ns		880		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling				mA	
(Fast page mode)		tpc = tpc (MIN.)	trac = 70 ns		920		3, 4, 6
		10 = 0 IIIA	trac = 80 ns		800		3, 4, 0
			trac = 100 ns		680		
CAS before RAS	Iccs	RAS Cycling					
refresh current		trc = trc (MIN.)	trac = 70 ns		1,120	mA	3, 4
		10 = 0 MA	trac = 80 ns		1,000	IIIA	3, 4
			trac = 100 ns		880		
Input leakage current	li (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10	+10	μΑ	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μА	
High level output voltage	Vон	lo = -5.0 mA		2.4		٧	
Low level output voltage	Vol	lo = +4.2 mA			0.4	V	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-421000A32 series]

		trac =	60 ns	trac =	70 ns	TRAC =	80 ns	trac =	100 ns		
Parameter	Symbol		MAX.		MAX.		MAX.		MAX.	Unit	Notes
Read/Write Cycle Time	trc	120		140		160		190		ns	
Fast Page Mode Cycle Time	tec	40		45		50		60		ns	
Access Time from RAS	trac		60		70		80 .		100	ns	10, 11
Access Time from CAS	tcac		15		20		20		25	ns	10, 11
Access Time Column Address	taa		30		35		40		50	ns	10, 11
Access Time from CAS Precharge	tacp		35		40		45		55	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	17	50	ns	10
CAS to Data Setup Time	tclz	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time	t RP	50		60		′70		80		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	100	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t RASP	60	125,000	70	125,000	80	125,000	100	125,000	ns	
RAS Hold Time	trish	20		20		20		25		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	25	10,000	ns	
CAS Hold Time	tcsн	60		70		80		100		ns	
RAS to CAS Delay Time	trco	20	40	20	50	25	60	25	75	ns	10
CAS to RAS Precharge Time	tcrp	10		10		10		10		ns	13
CAS Precharge Time	tcpn	10		10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		10		ns	
RAS Precharge CAS Hold Time	TRPC	10		10		10		10		ns	
RAS Hold Time from CAS Precharge	TRHCP	35		40		45		55		ns	
Row Address Setup Time	tasa	0		0		0		0		ns	
Row Address Hold Time	trah	10		10		12		12		ns	
Column Address Setup Time	tasc	0		0		0		0		ns	
Column Address Hold Time	tcan	15		15		15		20		ns	
Column Address Lead Time Referenced to RAS	tRAL	30		35		40		50		ns	
Read Command Setup Time	trcs	0		0		0		0		ns	
Read Command Hold Time Referenced to RAS	tran	10		10		10		10		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		0		ns	14
WE Hold Time Referenced to CAS	twcH	15		15		15		20		ns	15
Data-in Setup Time	tos	0		0		0		0		ns	16
Data-in Hold Time	tон	15		15		15		20		ns	16
Write Command Setup Time	twcs	0		0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsn	10		10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	15		15		15		20		ns	
WE Setup Time	twsr	10		10		10		10		ns	
WE Hold Time	twnr	15		15		15		20		ns	
Refresh Time	tref		16		16		16		16	ms	



[MC-421000A36 series]

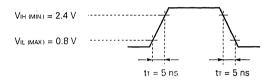
		trac =	70 ns	trac =	80 ns	trac =	100 ns		
Parameter	Symbol	MIN.	MAX.		MAX.		MAX.	Unit	Notes
Read/Write Cycle Time	trc	140		160		190		ns	
Fast Page Mode Cycle Time	tpc	45		50		60		ns	
Access Time from RAS	TRAC		70		80		100	ns	10, 11
Access Time from CAS	tcac		20		20		25	ns	10, 11
Access Time Column Address	taa		35		40		50	ns	10, 11
Access Time from CAS Precharge	tace		40		45		55	ns	11
RAS to Column Address Delay Time	trad	15	35	17	40	17	50	ns	10
CAS to Data Setup Time	tcız	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	trp	60		70		80		ns	
RAS Pulse Width	tras	70	10,000	80	10,000	100	10,000	ns	
RAS Pulse Width (Fast Page Mode)	TRASP	70	125,000	80	125,000	100	125,000	ns	
RAS Hold Time	trsh	20		20		25		ns	
CAS Pulse Width	tcas	20	10,000	20	10,000	25	10,000	ns	
CAS Hold Time	tсsн	70		80		100		ns	
RAS to CAS Delay Time	trco	20	50	25	60	25	75	ns	10
CAS to RAS Precharge Time	tcrp	10		10		10		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	10		10		10		ns	
RAS Hold Time from CAS Precharge	trhcp	40		45		55		ns	
Row Address Setup Time	tasr	0		0		0		ns	
Row Address Hold Time	trah	10		12		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	17		20		20		ns	
Column Address Lead Time Referenced to RAS	tral	35		40		50		ns	
Read Command Setup Time	trics	0		0		0		ns	
Read Command Hold Time Referenced to RAS	tarh	10		10		10		ns	14
Read Command Hold Time Referenced to CAS	trcH ,	0		0		0		ns.	14
WE Hold Time Referenced to CAS	twch	15		15		20		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	15		20		20		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsn	10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	15		15		20		ns	
WE Setup Time	twsn	10		10		10		ns	
WE Hold Time	twnn	15		15		20		ns	
Refresh Time	tref		16		16		16	ms	



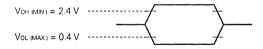
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- 7. Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (MAX.)	trad + taa (MAX.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions $trad \ge trad (MAX.)$ and $trad \ge trad (MAX.)$ will not cause any operation problems.

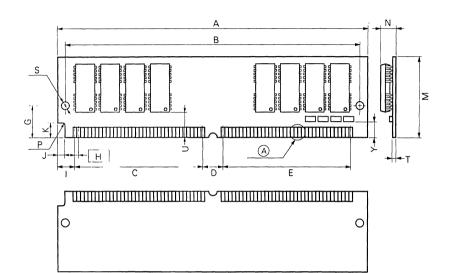
- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (мах.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voн or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

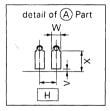
Timing Chart

Please refer to Timing Chart 2, page 375.

Package Drawings

[MC-421000A32B, 421000A32F]

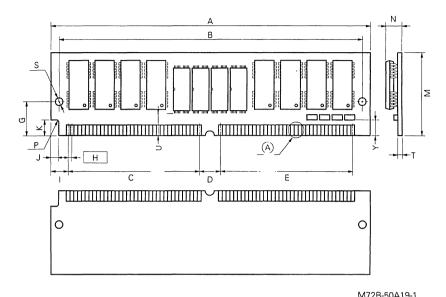


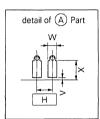


		M72B-50A21-1
ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44 45	1.750
D	6.35	0.250
Е	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
_	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
Z	5.08 MAX.	0.200 MAX.
Р	R 2.0	R 0.079
S	ø3.18	ø0.125
Т	1.27-0.08	0.050±0.004
U	6.5 MIN.	0.255 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Υ	3.75 MIN.	0.147 MIN.



(Not Applicable)

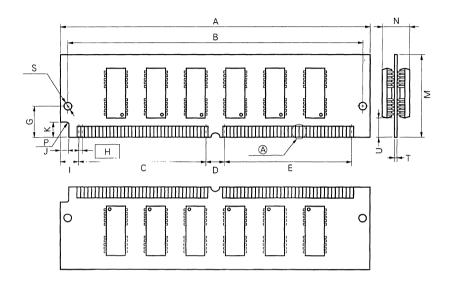


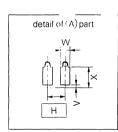


ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
N	5.08 MAX.	0.200 MAX.
Р	R 2.0	R 0.079
S	ø3.18	φ0.125
Т	1.27 ^{+0.1} _{-0.08}	0.050±0.004
U	5.32 MIN.	0.209 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Υ	3.75 MIN.	0.147 MIN.



[MC-421000A36BE, 421000A36FE]

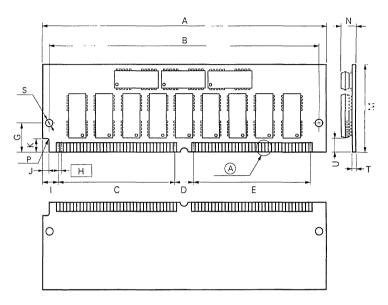


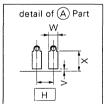


		M72B-50A33-1
ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
1	6.35	0.250
J	2.03	0.080
K,	6.35	0.250
М	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Р	R 1.57	R 0.062
S	Ø3.18	φ0.125
Т	1.27-0 08	0.050±0.004
U	6.0 MIN.	0.236 MIN.
V _.	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.



[MC-421000A36BJ, 421000A36FJ]





		M72B-50A23-2
ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
Е	44.45	1.750
G	10.16	0 400
H	1.27 (T.P.)	0.050 (T.P.)
-	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	31.75	1 250
N	5.08 MAX.	0.200 MAX.
Р	R 2.0	R 0.079
S	ø3.18	Ø0.125
T	1.27+0.1	0.050±0.004
U	3.78 MIN.	0.148 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
Х	2.54 MIN.	0.100 MIN.



DATA SHEET



MOS INTEGRATED CIRCUIT MC-422000A32BA, 422000A32FA

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000A32BA, 422000A32FA are 2,097,152 words by 32 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μ PD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surfacemounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- · 2,097,152 words by 32 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time	Power consumption (MAX.)		
·	(MAX.)	(MIN.)	Active	Standby	
MC-422000A32-60	60 ns	110 ns	1,782 mW	00	
MC-422000A32-70	70 ns	130 ns	1,672 mW	22 mW	
MC-422000A32-80	80 ns	150 ns	1,562 mW	(CMOS level input)	

- · 1,024 refresh cycles/16 ms
- · CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)



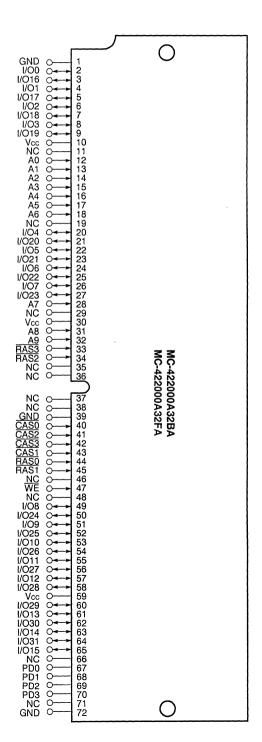
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32BA-60	60 ns	72-pin Single In-line Memory Module	4 pieces of μPD4218160LE
MC-422000A32BA-70	70 ns	(Socket Type)	(400 mil SOJ)
MC-422000A32BA-80	80 ns	Edge connector: Solder coating (HAL)	[Double side]
MC-422000A32FA-60	60 ns	72-pin Single In-line Memory Module	[Double side]
MC-422000A32FA-70	70 ns	(Socket Type)	
MC-422000A32FA-80	80 ns	Edge connector: Gold plating	



Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



 I/O0 - I/O31
 : Data Inputs/Outputs

 CAS0 - CAS3
 : Column Address Strobe

 RAS0 - RAS3
 : Row Address Strobe

 WE
 : Write Enable

 Vcc
 : Power Supply

 GND
 : Ground

: Address Inputs

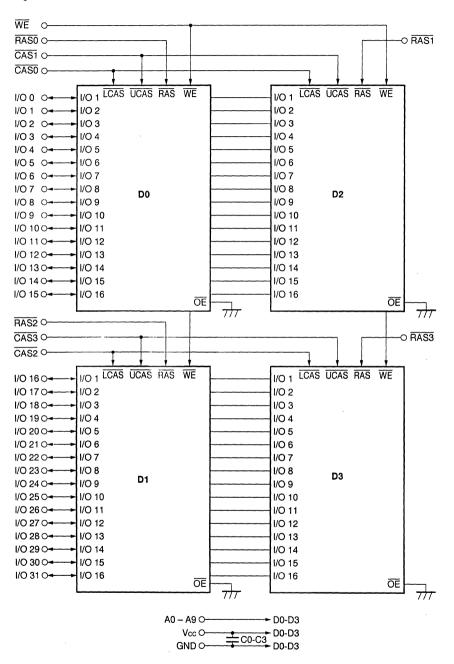
NC : No connection

A0 - A9

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	,	Access Time	е
Name	No.	60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Remark D0 - D3: μPD4218160



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vī		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Po		4	w
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.5	5.0	5.5	٧
High level input voltage	ViH		2.4		Vcc + 1.0	V
Low level input voltage	VıL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance ($T_A = 25$ °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A9			40	
	C ₁₂	WE			48	
	Сіз	RASO - RAS3			22	pF
	C14	CASO - CAS3			29	
Data Input/Output capacitance	C _{I/O}	1/00 - 1/031			26	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling	trac = 60 ns		324		
	1	trc = trc (MIN.)	trac = 70 ns		304	mA	3, 4, 7
		lo = 0 mA	trac = 80 ns		284		
Standby current	lcc2	RAS, CAS ≥ VIH (MIN.)	lo = 0 mA		8	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		4	111/4	
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		324		
		$\overline{CAS} \ge V_{\text{IH (MIN.)}}$ $t_{RC} = t_{RC \text{ (MIN.)}}$	trac = 70 ns		304	mA	3, 4, 5, 7
		Io = 0 mA	trac = 80 ns		284		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		184		
(Fast page mode)		tec = tec (MIN)	trac = 70 ns		164	mA	3, 4, 6
		Io = 0 mA	trac = 80 ns		144		
CAS before RAS	loos	RAS Cycling	trac = 60 ns		324		
refresh current		tric = tric (MIN.)	trac = 70 ns		304	mA	3, 4
		Io = 0 mA	trac = 80 ns		284		
Input leakage current	lı (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10	+10	μΑ	
Output leakage current	lo (t)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μΑ	
High level output voltage	Vон	lo :: −2.5 mA		2.4		٧	
Low level output voltage	Vol	lo = +2.1 mA			0.4	٧	



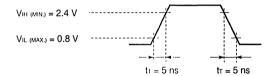
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

		trac	= 60 ns	trac	= 70 ns	trac	= 80 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	tric	110		130		150		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		15		20		20	ns	10, 11
Access Time Column Address	taa		30		35		40	ns	10, 11
Access Time from CAS Precharge	tace		35		40		45	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	tт	3	50	3	50	3	50	ns	
RAS Precharge Time	tap	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tязн	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	torp	5		5		5		ns	13
CAS Precharge Time	topn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	top	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	5		5		5		ns	
RAS Hold Time from CAS Precharge	trhcp	35		40		45		ns	
Row Address Setup Time	tasa	0		0		0		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	t CAH	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	t ran	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	tпсн	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	tref		16		16		16	ms	

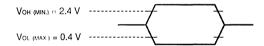


Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tac and tac).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- 7. lcc1 and lcc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition
 - (1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	trac (MAX.)	trac (max.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trod + toac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trad, that or toac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trich (MIN.) or trich (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

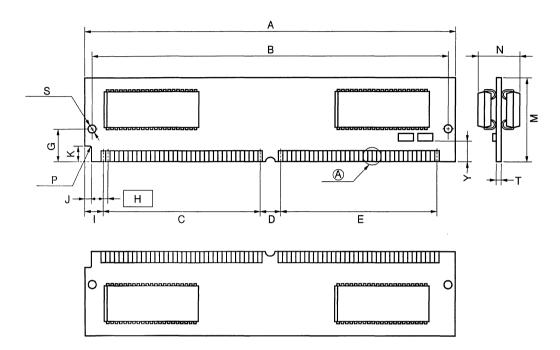
Timing Chart

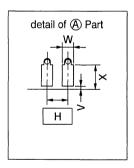
Please refer to Timing Chart 1, page 365.



Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
Е	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
1	6.35	0.250
J	2.03	0.080
К	6.35	0.250
М	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Р	R1.57	R0.062
S	φ3.18	ϕ 0.125
Т	1.27+0.1	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.
		MZOD FOA45

M72B-50A45



MOS INTEGRATED CIRCUIT MC-422000A32, 422000A36 SERIES

2 M-WORD BY 32-BIT, 2 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000A32 series is a 2 097 152 words by 32 bits dynamic RAM module on which 16 pieces of 4 M DRAM (µPD424400) are assembled.

The MC-422000A36 series is a 2 097 152 words by 36 bits dynamic RAM module on which 16 pieces of 4 M DRAM (μ PD424400) and 8 pieces of 1 M DRAM (μ PD421000) are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2 097 152 words by 32 bits organization (MC-422000A32 series)
- 2 097 152 words by 36 bits organization (MC-422000A36 series)
- Fast access and cycle time

Family	Access time	R/W cycle time	Power cor	
,,	(MAX.) (MIN.)		Active	Standby
MC-422000A32-60	60 ns	120 ns	5 355 mW	
MC-422000A32-70	70 ns	140 ns	4 515 mW	
MC-422000A32-80	80 ns	160 ns	4 095 mW	84 mW
MC-422000A32-10	100 ns	190 ns	3 675 mW	
MC-422000A36-70	70 ns	140 ns	6 195 mW	
MC-422000A36-80	80 ns	160 ns	5 565 mW	126 mW
MC-422000A36-10	100 ns	190 ns	4 935 mW	

- 1 024 refresh cycles/16 ms
- Three refresh modes are available: CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- All inputs and outputs are TTL compatible
- Single +5.0 V ± 5 % power supply
- Access time can be distinguished with characteristics of PD-pins(PD0 to PD3)

The information in this document is subject to change without notice.



Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32B-60	60 ns	70 . 0. 1 . 1	
MC-422000A32B-70	70 ns	72-pin Single In-line Memory Module	
MC-422000A32B-80	80 ns	(Socket Type) Edge connector : Solder coating (HAL)	16 pieces of µPD424400LA
MC-422000A32B-10	100 ns	Lago commenter : Donast counting (1 // L2)	(300 mil SOJ)
MC-422000A32F-60	60 ns		
MC-422000A32F-70	70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	[Double side]
MC-422000A32F-80	80 ns		
MC-422000A32F-10	100 ns	Lage connector . Gold plating	
MC-422000A36BJ-70 MC-422000A36BJ-80 MC-422000A36BJ-10	70 ns 80 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	16 pieces of μPD424400LA (300 mil SOJ) 8 pieces of μPD421000LA
		72-pin Single In-line Memory Module	(300 mil SOJ)
MC-422000A36FJ-70	70 ns	(Socket Type)	[Double side]
MC-422000A36FJ-80	80 ns	Edge connector : Gold plating	
MC-422000A36FJ-10	100 ns		

Quality Grade

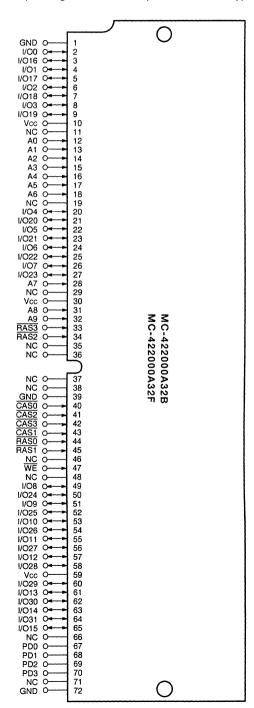
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Front view)

[MC-422000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0-A9 : Address Inputs

1/00-1/031 : Data Inputs/Outputs

CAS0-CAS3 : Column Address Strobe

RAS0-RAS3 : Row Address Strobe

: Ground

WE : Write Enable

: Power Supply

Vcc

GND

NC : No connection

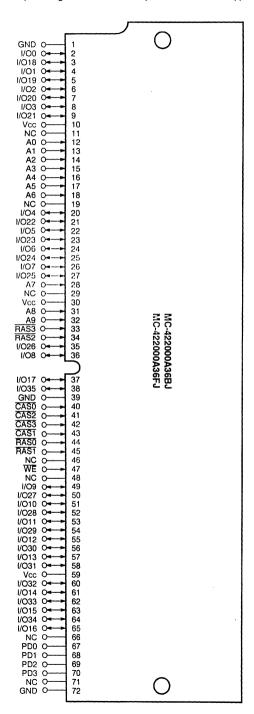
The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	Access Time						
Name	No.	60 ns	70 ns	80 ns	100 ns			
PD0	67	NC	NC	NC	NC			
PD1	68	NC	NC	NC	NC			
PD2	69	NC	GND	NC	GND			
PD3	70	NC	NC	GND	GND			



[MC-422000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0-A9 :

: Address Inputs

1/00-1/035

: Data Inputs/Outputs

CAS0-CAS3

: Column Address Strobe

RAS0-RAS3

: Row Address Strobe

WE

: Write Enable

Vcc

: Power Supply

GND

: Ground

NC

: No connection

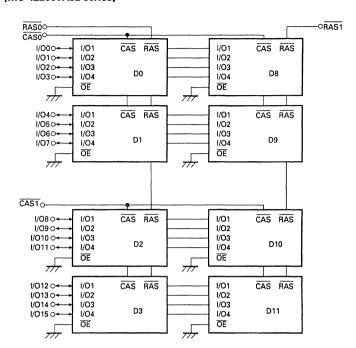
The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	Access Time					
Name	No.		70 ns	80 ns	100 ns		
PD0	67	NC	NC	NC	NC		
PD1	68	NC	NC	NC	NC		
PD2	69	NC	GND	NC	GND		
PD3	70	NC	NC	GND	GND		

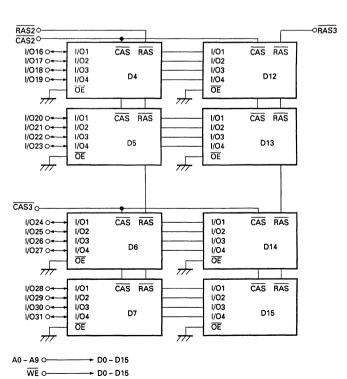


Block Diagrams

[MC-422000A32 series]



Remark D0-D15 : μPD424400



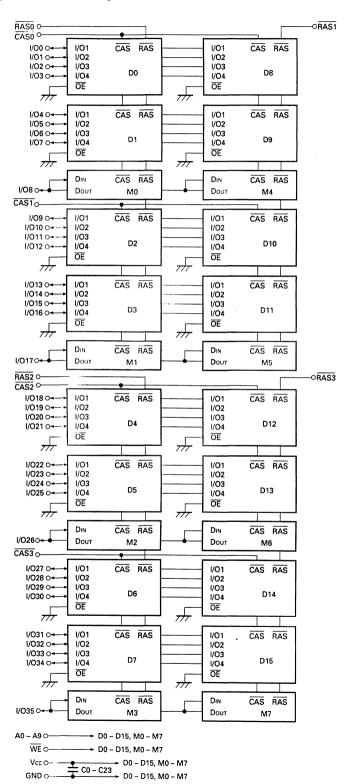
D0 - D15 = C0 - C15 D0 - D15

Vcc o

GND o-



[MC-422000A36 series]



Remark D0-D15 : μPD424400 M0-M7 : μPD421000



Electrical Specifications Notes 1, 2 **Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-1.0 to +7.0	٧
Supply voltage	Vcc		-1.0 to +7.0	V .
Output current	lo		50	mA
Dawar dissination	Po	MC-422000A32	16	10/
Power dissipation		MC-422000A36	24	W
Operating temperature	Topt		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	ViH		2.4		Vcc +1.0	٧
Low level input voltage	VıL		-1.0		+0.8	٧
Ambient temperature	Та		0		70	°C

Capacitance ($T_a = +25 \,^{\circ}\text{C}$, $f = 1 \,\text{MHz}$) [MC-422000A32 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
	C 1	A0 - A9			121	
	C12	WE			137	
Input capacitance	Сіз	RASO - RAS3			48	pF
	C14	CASO - CAS3			48	
Data Input/Output capacitance	C1/0	I/O0 - I/O31			29	pF

[MC-422000A36 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
	C11	A0 - A9			161	
14	C12	WE			193	
Input capacitance	Сіз	RASO - RAS3			62	pF
	C14	CASO - CAS3			62	
Data Input/Output capacitance	C1/01	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	C1/02	I/O8, I/O17, I/O26, I/O35			39	



DC Characteristics (Recommended Operating Conditions unless otherwise noted) [MC-422000A32 series]

Parameter	Symbol	Test condition			MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling trc = trc(MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns trac = 100 ns		1 020 860 780 700	m A	3,4,7
Standby current	Icc 2	\overline{RAS} , $\overline{CAS} \ge V_{IH (MIN.)}$ \overline{RAS} , $\overline{CAS} \ge V_{CC-0.2} V$	lo = 0 mA		32 16	mA	
RAS only refresh current	Іссз	RAS Cycling CAS ≥ VIH (MIN.) trc = trc(MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns trac = 100 ns		1 020 860 780 700	mA	3,4,5,7
Operating current (Fast page mode)	Icc4	RAS ≤ VIL (MAX.), CAS Cycling tpc = tpc(MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns trac = 100 ns		780 700 620 540	mA	3,4,6
CAS before RAS refresh current	lcc5	RAS Cycling trc = trc(MIN.) lo = 0 mA	tRAC = 60 ns $tRAC = 70 ns$ $tRAC = 80 ns$ $tRAC = 100 ns$		1 020 860 780 700	mA	3,4
Input leakage current	lı (L)	VI = 0 to 5.5 V all other pins not under test = 0 V		-10	+10	μА	
Output leakage current	lo(L)	I/O0 to I/O31 is disabled (Hi-Z) Vo = 0 to 5.5 V		-10	+10	μΑ	
High level output voltage	Vон	lo = -5.0 mA		2.4		V	
Low level output voltage	Vol	10 = +4.2 mA			0.4	V	



[MC-422000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling trc = trc(MIN.) lo = 0 mA	trac = 70 ns trac = 80 ns trac = 100 ns		1 180 1 060 940	mA	3,4,7
Standby current	Icc2	\overline{RAS} , $\overline{CAS} \ge V$ IH (MIN.) \overline{RAS} , $\overline{CAS} \ge V$ CC-0.2 V	lo = 0 mA		48	mA	
RAS only refresh current	lcc3	RAS Cycling CAS ≥ VIH (MIN.) trc = trc(MIN.) lo = 0 mA	trac = 70 ns trac = 80 ns trac = 100 ns		1 180 1 060 940	mA	3,4,5,7
Operating current (Fast page mode)	Icc4	RAS ≤ VIL (MAX.), CAS Cycling tpc = tpc(MIN.) Io = 0 mA	trac = 70 ns trac = 80 ns trac = 100 ns		980 860 740	mA	3,4,6
CAS before RAS refresh current	lcc5	RAS Cycling trc = trc(MIN.) lo = 0 mA	trac = 70 ns trac = 80 ns trac = 100 ns		1 180 1 060 940	mA	3,4
Input leakage current	lı (L)	VI = 0 to 5.5 V all other pins not under test = 0 V		-10	+10	μΑ	
Output leakage current	lo(L)	I/O0 to I/O35 is disabled (Hi-Z) Vo = 0 to 5.5 V		-10	+10	μА	
High level output voltage	Vон	lo = -5.0 mA		2.4		V	
Low level output voltage	Vol	10 = +4.2 mA			0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9, 18

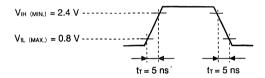
Danis de la		Symbol	trac=	60 ns	trac=	= 70 ns	trac =	80 ns	trac =	= 100 ns	l lmir	Note
Parameter		Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	NOTE
Read or Write Cycle Time		t RC	120		140		160		190		ns	
Fast Page Mode Cycle Time (Rea	d or Write)	t PC	40		45		50		60		ns	
Access Time from RAS		t RAC		60		70		80		100	ns	10,1
Access Time from CAS (Falling Edge)	MC-422000A32 MC-422000A36	tCAC		15		20		20		25	ns	10,1
Access Time from Column Addre	ess	taa		30		35		40	-	50	ns	10,1
Access Time from CAS Precharg	je	t ACP		35		40		45		55	ns	11
RAS to Column Address Delay T	ime	trad	15	30	15	35	17	40	17	50	ns	10
CAS to Data Setup Time		tclz	0	i	0		0		0		ns	11
Output Buffer Turn-off Delay Tim	ne (CAS)	toff	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)		tт	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time		trp	50		60		70		80		ns	
RAS Pulse Width (Random Read	, Write Cycle)	tras	60	10 000	70	10 000	80	10 000	100	10 000	ns	
RAS Pulse Width (Fast Page Mod		trasp		125 000	70	125 000	80	125 000		125 000	ns	
RAS Hold Time		trsh	20		20		20		25		ns	
CAS Pulse Width		tcas	20	10 000	20	10 000	20	10 000		10 000	ns	
CAS Hold Time		tcsн	60		70		80		100		ns	
RAS to CAS Delay Time	MC-422000A32 MC-422000A36	trcd	20	40	20	50	25	60	25	90 75	ns	10
CAS to RAS Precharge Time	1110 1220007 100	tcrp	10		10		10		10		ns	13
CAS Precharge Time		tcpn	10		10		10		10		ns	''
CAS Precharge Time (Fast Page	Mode)	tCP	10		10		10		10		ns	-
RAS Precharge CAS Hold Time		t RPC	10		10		10		10		ns	
RAS Hold Time from CAS Prech	arge	TRHCP	35		40		45		55		ns	
Row Address Setup Time		tasr	0		0		0		0		ns	-
Row Address Hold Time		trah	10		10		12		12		ns	
Column Address Setup Time		tasc	0		0		0		0		ns	
October 1	MC-422000A32				15		15					
Column Address Hold Time	MC-422000A36	tcah	15		17		20		20		ns	
Column Address Lead Time Refe		TRAL	30		35		40		50		ns	
Read Command Setup Time	7011000 10 11/10	trcs	0		0		0		0		ns	_
Read Command Hold Time Refe	renced to BAS	trrh	10		10		10		10		ns	14
Read Command Hold Time Refe		trch	0		0		0		0		ns	14
Write Command Hold Time Referenced to CAS		twch	15		15		15		20		ns	15
Data-in Setup Time		tos	0		0		0		0		ns	16
	MC-422000A32				0		15		-			10
Data-in Hold Time	MC-422000A36	ton	15		15		20		20		ns	16
Write Command Setup Time		twcs	0		0		0		0		ns	17
CAS Setup Time for CAS before	RAS Refresh	tcsr	10		10				10		ns	''
CAS Hold Time for CAS before F		tchr			15		10 15				ns	-
WE Setup Time		twsn	15 10		10		10		20			-
			10		10		10		10		ns	<u> </u>
WE Hold Time	WE Hold Time		15		15		15	1	20		ns	



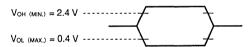
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tac and tec).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume tr = 5 ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \le t_{RAD} (MAX.), t_{RCD} \le t_{RCD} (MAX.)$	TRAC (MAX.)	TRAC (MAX.)
$t_{RAD} > t_{RAD} (MAX.), t_{RCD} \leq t_{RCD} (MAX.)$	TAA (MAX.)	trad + taa (Max.)
trcd > trcd (MAX.)	t CAC (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and tradimax.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or tax) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trade \geq trade (MAX.) will not cause any operation problems.

- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirement should be applied for RAS / CAS cycles preceded by any cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
- 18. The column "trac = 60 ns" is not applicable to MC-422000A36.

Timing Chart

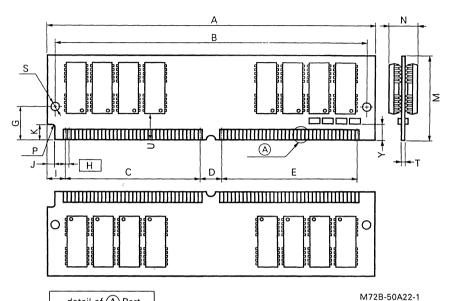
Please refer to Timing Chart 2, page 375.

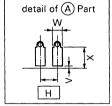


Package Drawings

MC-422000A32B, 422000A32F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

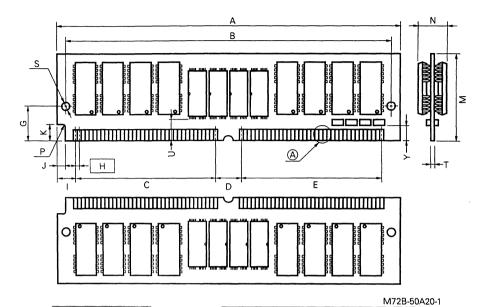


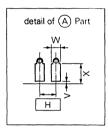


ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
Κ	6.35	0.250
М	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Р	R 2.0	R 0.079
S	ø3.18	Ø0.125
Т	1.27-0 08	0.050±0.004
U	6.5 MIN.	0.255 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Υ	3.75 MIN.	0.147 MIN.

(Not Applicable)

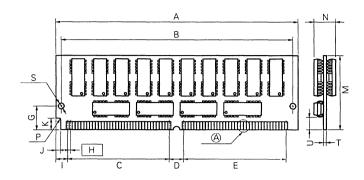
72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

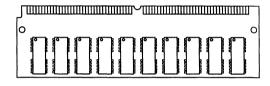


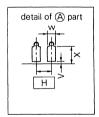


ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
C	44.45	1.750
D	6.35	0.250
Е	44.45	1.750
G	10.16	0.400
Η	1.27 (T.P.)	0.050 (T.P.)
_	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
N	9.0 MAX.	0.354 MAX.
Р	R 2.0	R 0.079
S	ø3.18	ø0.125
Т	1.27 ^{+0.1} _{-0.08}	0.050±0.004
C	5.32 MIN.	0.209 MIN.
. V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
Х	2.54 MIN.	0.100 MIN.
Υ	3.75 MIN.	0.147 MIN.

MC-422000A36BJ, 422000A36FJ 72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)







		M72B-50A44
ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
1	6.35	0.250
J	2.03	0.080
Κ	6.35	0.250
М	31.75	1.250
N	9.0 MAX.	0.355 MAX.
Р	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 +0 1 08	0.050±0.004
U	3.17 MIN.	0.124 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
Х	3.15 MIN.	0.124 MIN.





MOS INTEGRATED CIRCUIT MC-424000A32, 424000A36 SERIES

4 M-WORD BY 32-BIT, 4 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-424000A32 series is a 4,194,304 words by 32 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μ PD4217400 are assembled.

The MC-424000A36 series is a 4,194,304 words by 36 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μ PD4217400 and 4 pieces of 4 M DRAM: μ PD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 32 bits organization (MC-424000A32 series)
- 4,194,304 words by 36 bits organization (MC-424000A36 series)
- · Fast access and cycle time

Family	Access time	R/W cycle time	Power consumption (MAX.)			
	(MAX.)	(MIN.)	Active	Standby		
MC-424000A32-60	60 ns	110 ns	4,840 mW			
MC-424000A32-70	70 ns	130 ns	4,400 mW	44 mW (CMOS level input)		
MC-424000A32-80	80 ns	150 ns	3,960 mW	(CiviO3 level input)		
MC-424000A36-60	60 ns	110 ns	7,480 mW			
MC-424000A36-70	70 ns	130 ns	6,600 mW	66 mW (CMOS level input)		
MC-424000A36-80	80 ns	150 ns	5,940 mW	(Civios level input)		

- · 2,048 refresh cycles/32 ms
- · 2,048 refresh cycles/16 ms (MC-424000A36 burst refesh)
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.



Ordering Information

[MC-424000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A32B-60	60 ns	72-pin Single In-line Memory Module	8 pieces of μPD4217400LA
MC-424000A32B-70	70 ns	(Socket Type)	(300 mil SOJ)
MC-424000A32B-80	80 ns	Edge connector: Solder coating (HAL)	[Single side]
MC-424000A32F-60	60 ns	72-pin Single In-line Memory Module	
MC-424000A32F-70	70 ns	(Socket Type)	
MC-424000A32F-80	80 ns	Edge connector: Gold plating	

[MC-424000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A36BE-60	60 ns	72-pin Single In-line Memory Module	8 pieces of μPD4217400LA
MC-424000A36BE-70	70 ns	(Socket Type)	(300 mil SOJ)
MC-424000A36BE-80	80 ns	Edge connector: Solder coating (HAL)	4 pieces of μPD424100LA (300 mil SOJ)
MC-424000A36FE-60	60 ns	72-pin Single In-line Memory Module	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
MC-424000A36FE-70	70 ns	(Socket Type)	[Double side]
MC-424000A36FE-80	80 ns	Edge connector: Gold plating	
MC-424000A36BJ-60	60 ns	72-pin Single In-line Memory Module	8 pieces of μPD4217400LA
MC-424000A36BJ-70	70 ns		(300 mil SOJ)
MC-424000A36BJ-80	80 ns	Edge connector: Solder coating (HAL)	4 pieces of μPD424100LA (300 mil SOJ)
MC-424000A36FJ-60	60 ns	72-pin Single In-line Memory Module	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
MC-424000A36FJ-70	70 ns	(Socket Type)	[Single side]
MC-424000A36FJ-80	80 ns	Edge connector: Gold plating	

Quality Grade

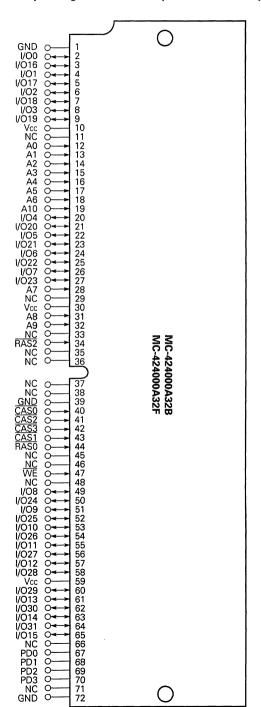
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

[MC-424000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0 - A10 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
CASO - CAS3 : Column Address Strobe
RAS0, RAS2 : Row Address Strobe

 WE
 : Write Enable

 Vcc
 : Power Supply

 GND
 : Ground

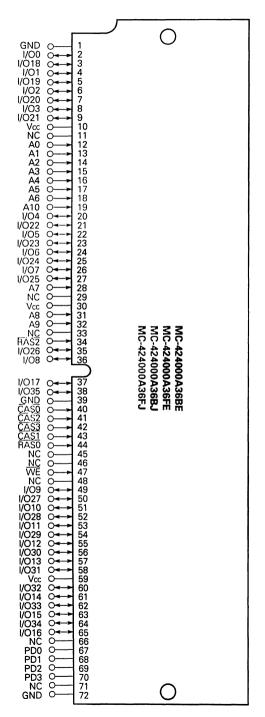
 NC
 : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD0	67	GND	GND	GND		
PD1	68	NC	NC	NC		
PD2	69	NC	GND	NC		
PD3	70	NC	NC	GND		



[MC-424000A36 series]
72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



 A0 - A10
 : Address Inputs

 I/O0 - I/O35
 : Data Inputs/Outputs

 CAS0 - CAS3
 : Column Address Strobe

 RAS0, RAS2
 : Row Address Strobe

 WE
 : Write Enable

GND : Ground
NC : No connection

Vcc

The internal connection of PD pins (PD0 to PD3) depends on access time.

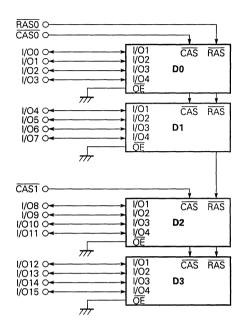
: Power Supply-

Pin	Pin Pin		Access Time				
Name	No.	60 ns	70 ns	80 ns			
PD0	67	GND	GND	GND			
PD1	68	NC	NC	NC			
PD2	69	NC	GND	NC			
PD3	70	NC	NC	GND			

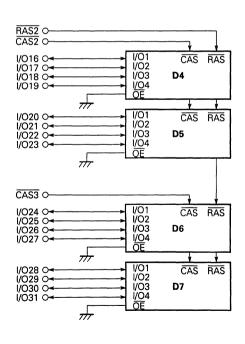


Block Diagram

[MC-424000A32 series]

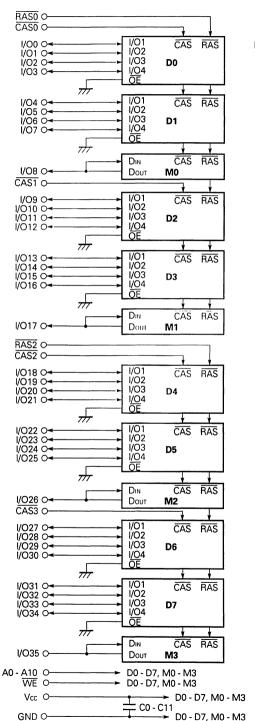


Remark D0 - D7 : μPD4217400





[MC-424000A36 series]



Remark D0 - D7 : μ PD4217400 M0 - M3 : μ PD424100



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-1.0 to +7.0	٧
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Pp MC-424000A32		8	
		MC-424000A36	12	W
Operating temperature	Topt		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.5	5.0	5.5	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Ambient temperature	Ta		0		70	°C

Capacitance ($T_a = +25$ °C, f = 1 MHz) [MC-424000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cn	A0 - A10			68	
	Cı2	WE			76	_
	Сіз	RASO, RASZ			43	pF
	C14	CASO - CAS3			29	
Data Input/Output capacitance	Ci/o	1/00 - 1/031			17	pF

[MC-424000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Сп	A0 - A10			88	
	Ci2	WE			104	_
	Сіз	RASO, RAS2			57	pF
	C ₁₄	CASO - CAS3			36	
Data Input/Output capacitance	C _{I/O1}	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	C1/02	I/O8, I/O17, I/O26, I/O35			22	



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-424000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling	trac = 60 ns		880		
		trc = trc (MIN.)	trac = 70 ns		800	mA	3, 4, 7
		10 = U MA	trac = 80 ns		720		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		16	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		8		
RAS only refresh current	lcc3	RAS Cycling	trac = 60 ns		880		
		TAS ≥ Vih (MIN.)	trac = 70 ns		800	mA	3, 4, 5, 7
		lo = 0 mA	trac = 80 ns		720		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		560		
(Fast page mode)			trac = 70 ns		480	mA	3, 4, 6
		lo = 0 mA	trac = 80 ns		400		
CAS before RAS	lccs	RAS Cycling	trac = 60 ns		880		
refresh current		trc = trc (MIN.)	trac = 70 ns		800	mA	3, 4
		lo = 0 mA	trac = 80 ns		720]
Input leakage current	lino	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10	+10	μΑ	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μΑ	
High level output voltage	Vон	lo = -5.0 mA		2.4		٧	
Low level output voltage	Vor	lo = +4.2 mA			0.4	٧	



[MC-424000A36 series]

Parameter	Symbol	Test condition	1	MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling	trac = 60 ns		1,360		
		lo = 0 mA	trac = 70 ns		1,200	mA	3, 4, 7
		10 - 0 11111	trac = 80 ns		1,080		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		24	mA	
		RAS, CAS ≥ Vcc - 0.2 V	1o = 0 mA		12		
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		1,360		
		CAS ≥ Vih (MIN.) trc = trc (MIN.)	trac = 70 ns		1,200	mA	3, 4, 5, 7
		lo = 0 mA	trac = 80 ns		1,080		1
Operating current	Icc4	$\overline{RAS} \leq V_{IL (MAX.)}, \overline{CAS} Cycling$	trac = 60 ns		920		
(Fast page mode)		tpc = tpc (MIN.) lo = 0 mA	trac = 70 ns		800	mA	3, 4, 6
		10 = 0 IIIA	trac = 80 ns		680		
CAS before RAS	lccs	RAS Cycling	trac = 60 ns		1,360		
refresh current		trc = trc (MIN.) lo = 0 mA	trac = 70 ns		1,200	mA	3, 4
		10 = 0 IIIA	trac = 80 ns		1,080		}
Input leakage current	lı (L)	V _I = 0 to 5.5 V All other pins not under test = 0 V		-10	+10	μА	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μА	
High level output voltage	Vон	lo ≈ -5.0 mA		2.4		٧	
Low level output voltage	Vol	lo = +4.2 mA			0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-424000A32 series]

	trac = 60 ns trac =		RAC = 70 ns trac = 80 ns		= 80 ns	T			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Access Time from RAS	TRAC		60		70		80	ns	10, 11
Access Time from CAS	tcac		15		18		20	ns	10, 11
Access Time Column Address	taa		30		35		40	ns	10, 11
Access Time from CAS Precharge	tace		35		40		45	ns	11
RAS to Column Address Delay Time	TRAD	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcız	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	t RP	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	1
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tasa	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tcsii	60		70		80		ns	
RAS to CAS Delay Time	trco	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcap	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	5		5		5		ns	
RAS Hold Time from CAS Precharge	trhcp	35		40		45		ns	
Row Address Setup Time	tasa	0		0		0		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	tarn	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	tясн	0		0		0		ns	14
WE Hold Time Referenced to CAS	twcн	10		10		15		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsr	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tсня	10		10		10		ns	
WE Setup Time	twsn	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	tref		32		32		32	ms	



[MC-424000A36 series]

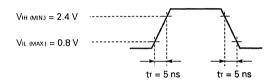
			TRAC	= 60 ns	trac	= 70 ns	TRAC	= 80 ns		Γ
Par	ameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time		trc	110		130		150		ns	
Fast Page Mode Cycle	e Time	tpc	40		45		50		ns	
Access Time from RA	us Vs	trac		60		70		80	ns	10, 11
Access Time from CA	<u></u>	tcac		15		20		20	ns	10, 11
Access Time Column	Address	taa		30		35		40	ns	10, 11
Access Time from CA	S Precharge	tace		35		40		45	ns	11
RAS to Column Addr	ess Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Ti	me	tcLz	0		0		0		ns	11
Output Buffer Turn-of	ff Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
Transition Time (Rise	and Fall)	tт	3	50	3	50	3	50	ns	
RAS Precharge Time		trp	40		50		60		ns	
RAS Pulse Width		tras	60	10,000	70	10,000	80	10,000	ns	1
RAS Pulse Width (Fas	st Page Mode)	TRASP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time		trsh	20		20		20		ns	
CAS Pulse Width		tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	The state of the s	tcsн	60		70		80		ns	
RAS to CAS Delay Tir	me	trco	20	40	20	50	25	60	ns	10
CAS to RAS Precharg	e Time	tcrp	10		10		10		ns	13
CAS Precharge Time		tcpn	10		10		10		ns	
CAS Precharge Time	(Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS I	Hold Time	trpc	10		10		10		ns	
RAS Hold Time from		trhcp	35		40		45		ns	
Row Address Setup T	ime	tasr	0		0		0		ns	
Row Address Hold Ti	me	trah	10		10		12		ns	
Column Address Setu	ıp Time	tasc	0		0		0		ns	
Column Address Hold	d Time	tcan	15		15		15		ns	
Column Address Lead	Time Referenced to RAS	TRAL	30		35		40		ns	
Read Command Setu	p Time	trcs	0		0		0		ns	
Read Command Hold	Time Referenced to RAS	taan	0		0		0		ns	14
Read Command Hold	Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Refere	WE Hold Time Referenced to CAS		15		15		15		ns	15
Data-in Setup Time		tos	0		0		0		ns	16
Data-in Hold Time		tон	15		15		15		ns	16
Write Command Setup Time		twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)		tcsr	10		10		10	`	ns	
CAS Hold Time (CAS before RAS Refresh)		tchr	10		10		10		ns	
WE Setup Time		twsr	10		10		10		ns	
WE Hold Time		twnr	15		15		15		ns	
Refresh Time	Distributed refresh	tref		32		32		32	ms	
	Burst refresh			16		16		16	ms	



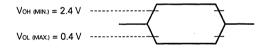
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. lcc1, lcc3, lcc4 and lcc5 depend on cycle rates (tRC and tPC).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t\tau = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS	
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)	
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	TAA (MAX.)	trad + taa (max.)	
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)	

trad (MAX.) and trcd (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad (MAX.) and trcd ≥ trcd (MAX.) will not cause any operation problems.

- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (мах.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voн or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tds (MIN.) and tdh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

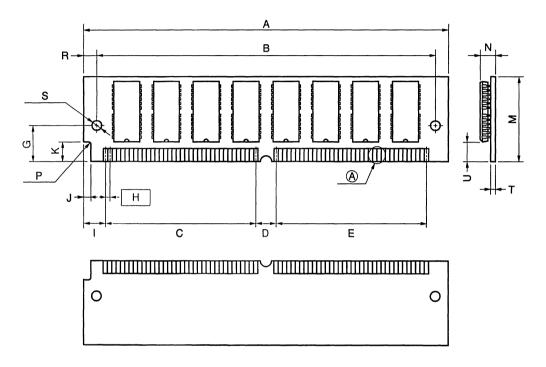
Timing Chart

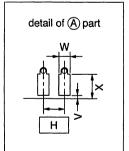
Please refer to Timing Chart 2, page 375.

Package Drawings

[MC-424000A32B, 424000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



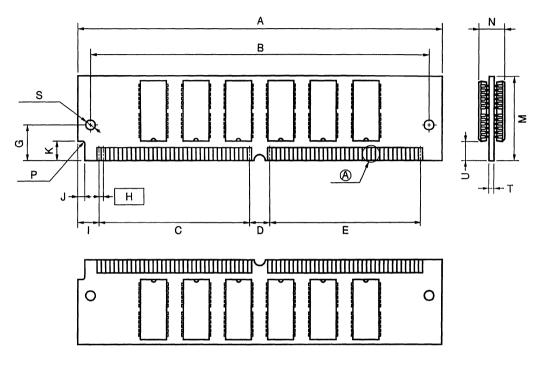


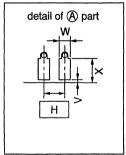
ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19±0.13	3.984 ^{+0.005}
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
R	3.38±0.13	0.133 ^{+0.006} -0.005
s	φ3.18	ϕ 0.125
Т	1.27 <u>+0.1</u> -0.08	0.050±0.004
U	5.5 MIN.	0.216 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A54

[MC-424000A36BE, 424000A36FE]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



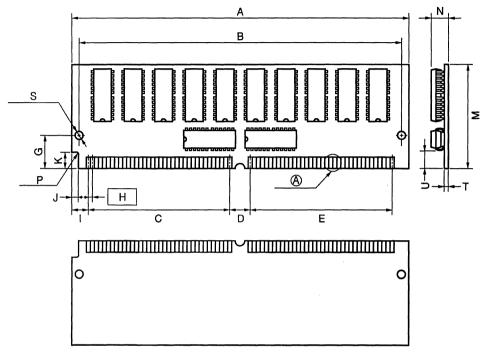


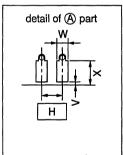
ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
Е	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Р	R1.57	R0.062
S	φ3.18	φ0.125
Т	1.27 ^{+0.1} -0.08	0.050±0.004
U	5.08 MIN.	0.200 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
Х	3.15 MIN.	0.124 MIN.
		M72B-50A47

M72B-50A47

[MC-424000A36BJ, 424000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES	
Α	107.95±0.13	4.250±0.006	
В	101.19	3.984	
С	44.45	1.750	
D	6.35	0.250	
E	44.45	1.750	
G	10.16	0.400	
Н	1.27 (T.P.)	0.050 (T.P.)	
l	6.35	0.250	
J	2.03	0.080	
K	6.35	0.250	
М	31.75	1.250	
N	5.08 MAX.	0.200 MAX.	
Р	R1.57	R0.062	
S	φ3.18	φ0.125	
Т	1.27 ^{+0.1} -0.08	0.050±0.004	
U	3.17 MIN.	0.124 MIN.	
V	0.25 MAX.	0.010 MAX.	
W	1.04±0.05	0.041±0.002	
Х	3.15 MIN. 0.124 MIN.		

M72B-50A51-1



MOS INTEGRATED CIRCUIT MC-428000A32, 428000A36 SERIES

8 M-WORD BY 32-BIT, 8 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-428000A32 series is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μ PD4217400 are assembled.

The MC-428000A36 series is a 8,388,608 words by 36 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μ PD4217400 and 8 pieces of 4 M DRAM: μ PD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 32 bits organization (MC-428000A32 series)
- 8,388,608 words by 36 bits organization (MC-428000A36 series)
- · Fast access and cycle time

Family	Access time	R/W cycle time	Power consumption (MAX.)		
	(MAX.)	(MIN.)	Active	Standby	
MC-428000A32-60	60 ns	110 ns	5,170 mW		
MC-428000A32-70	70 ns	130 ns	4,730 mW	88 mW (CMOS level input)	
MC-428000A32-80	80 ns	150 ns	4,290 mW	(Civios level iliput)	
MC-428000A36-60	60 ns	110 ns	7,810 mW		
MC-428000A36-70	70 ns	130 ns	6,930 mW	132 mW (CMOS level input)	
MC-428000A36-80	80 ns	150 ns	6,270 mW	Civios level lliput/	

- · 2,048 refresh cycles/32 ms
- 2,048 refresh cycles/16 ms (MC-428000A36 burst refesh)
- · CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.



Ordering Information

[MC-428000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A32B-60	60 ns	72-pin Single In-line Memory Module	16 pieces of μPD4217400LA
MC-428000A32B-70	70 ns	(Socket Type)	(300 mil SOJ)
MC-428000A32B-80	80 ns	Edge connector: Solder coating (HAL)	[Double side]
MC-428000A32F-60	60 ns	72-pin Single In-line Memory Module	
MC-428000A32F-70	70 ns	(Socket Type)	
MC-428000A32F-80	80 ns	Edge connector: Gold plating	

[MC-428000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A36BJ-60	60 ns	72-pin Single In-line Memory Module	16 pieces of μPD4217400LA
MC-428000A36BJ-70	70 ns	(Socket Type)	(300 mil SOJ)
MC-428000A36BJ-80	80 ns	Edge connector: Solder coating (HAL)	8 pieces of μPD424100LA (300 mil SOJ)
MC-428000A36FJ-60	60 ns	72-pin Single In-line Memory Module	1,000 11 0.00,
MC-428000A36FJ-70	70 ns	(Socket Type)	[Double side]
MC-428000A36FJ-80	80 ns	Edge connector: Gold plating	

Quality Grade

Standard

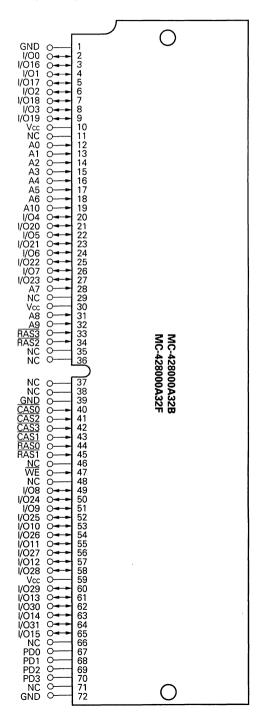
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.



Pin Configurations

[MC-428000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0 - A10 : Address Inputs

I/O0 - I/O31 : Data Inputs/Outputs

CAS0 - CAS3 : Column Address Strobe

RAS0 - RAS3 : Row Address Strobe

WE : Write Enable

Vcc : Power Supply

GND : Ground

NC : No connection

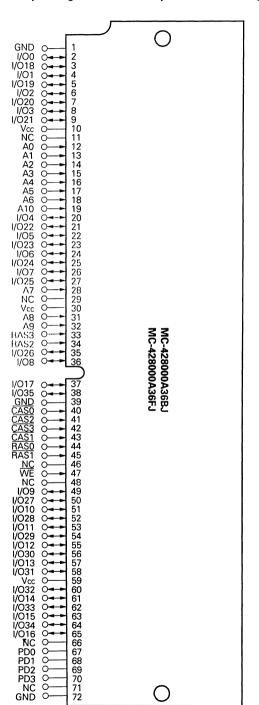
The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD0	67	NC	NC	NC		
PD1	68	GND	GND	GND		
PD2	69	NC	GND	NC		
PD3	70	NC	NC	GND		



[MC-428000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0 - A10 : Address Inputs

I/O0 - I/O35 : Data Inputs/Outputs

CAS0 - CAS3 : Column Address Strobe

RAS0 - RAS3 : Row Address Strobe

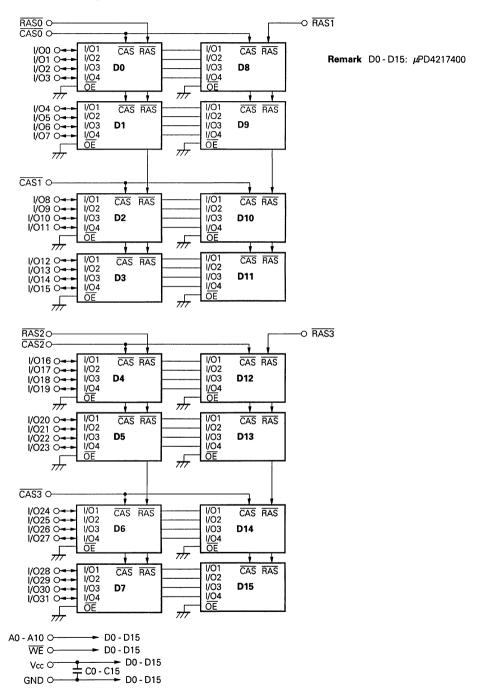
WE : Write Enable
Vcc : Power Supply.
GND : Ground
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin	Pin	,	Access Tim	e
Name	No.	60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

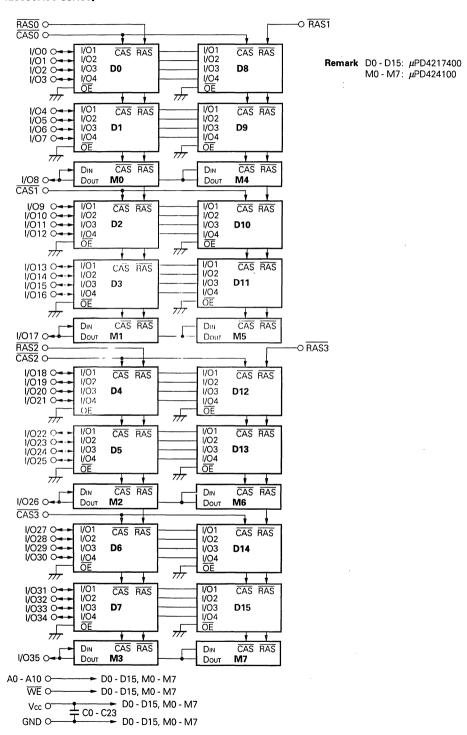
Block Diagrams

[MC-428000A32 series]





[MC-428000A36 series]





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	P⊳	MC-428000A32	16	
		MC-428000A36	24	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.5	5.0	5.5	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz) [MC-428000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A10			121	
	Cı2	WE			137	_
	Сіз	RASO - RAS3			48	pF
	C14	CASO - CAS3			48	
Data Input/Output capacitance	Ci/o	I/O0 - I/O31			29	pF

[MC-428000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A10			161	
	Cı2	WE			193	_
	Сіз	RASO - RAS3			62	pF
	Ci4	CASO - CAS3			62	
Data Input/Output capacitance	C _{1/01}	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	C1/O2	I/O8, I/O17, I/O26, I/O35			39	



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-428000A32 series]

Parameter	Symbol	Test condition	1	MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling	trac = 60 ns		940	,	
		lo = 0 mA	trac = 70 ns		860	mA	3, 4, 7
			trac = 80 ns		780		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		32	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		16		
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		940		,
		CAS ≥ ViH (MIN.) trc = trc (MIN.)	trac = 70 ns		860	mA	3, 4, 5, 7
		lo = 0 mA	trac = 80 ns		780		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		620		
(Fast page mode)		tpc = tpc (MIN.)	trac = 70 ns		540	mA	3, 4, 6
		10 L O IIIA	trac = 80 ns		460		
CAS before RAS	lccs	RAS Cycling	trac = 60 ns		940		
refresh current		trc = trc (MIN.)	trac = 70 ns		860	mA	3, 4
		10 = 0 HIA	trac = 80 ns		780		
Input leakage current	li (u)	V _I = 0 to 5.5 V All other pins not under tes	t = 0 V	-10	+10	μΑ	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μΑ	
High level output voltage	Vон	lo = -5.0 mA		2.4		٧	
Low level output voltage	Vol	lo = +4.2 mA			0.4	٧	



[MC-428000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc (MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns		1,420 1,260 1,140	mA	3, 4, 7
Standby current	Icc2	RAS, CAS ≥ VIH (MIN.) RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		48	mA	
RAS only refresh current	Іссз	RAS Cycling CAS ≥ Vih (MIN.) tac = tac (MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns		1,420 1,260 1,140	mA	3, 4, 5, 7
Operating current (Fast page mode)	lcc4	RAS VIL (MAX.), CAS Cycling tpc = tpc (MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns		980 860 740	mA	3, 4, 6
CAS before RAS refresh current	lcc5	RAS Cycling trc = trc (MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns		1,420 1,260 1,140	mA	3, 4
Input leakage current	lı (L)	V _I = 0 to 5.5 V All other pins not under tes	st = 0 V	-10	+10	μА	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μΑ	
High level output voltage	Vон	lo = -5.0 mA		2.4	0.4	V V	
Low level output voltage	Vol	lo = +4.2 mA			U.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-428000A32 series]

		trac	= 60 ns	trac	= 70 ns	trac	= 80 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Fast Page Mode Cycle Time	trc	40		45		50		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		15		18		20	ns	10, 11
Access Time Column Address	taa		30		35		40	ns	10, 11
Access Time from CAS Precharge	tacp		35		40		45	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	trp	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tлsн	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	5		5		5		ns	
RAS Hold Time from CAS Precharge	trhcp	35		40		45		ns	
Row Address Setup Time	tasr	0		0		0		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tсан	15		15		15		ns	
Column Address Lead Time Referenced to RAS	TRAL	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsr	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
WE Setup Time	twsr	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	tref		32		32		32	ms	



[MC-428000A36 series]

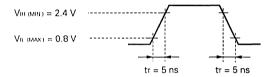
			trac	= 60 ns	trac	= 70 ns	TRAC	= 80 ns		
Par	ameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Tim	e	trc	110		130		150		ns	
Fast Page Mode Cycle	e Time	tpc	40		45		50		ns	
Access Time from RA	s	trac		60		70		80	ns	10, 11
Access Time from CA	<u> </u>	tcac		15		20		20	ns	10, 11
Access Time Column	Address	taa		30		35		40	ns	10, 11
Access Time from CA	S Precharge	tace		35		40		45	ns	11
RAS to Column Addre	ess Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Ti	me	tcLz	0		0		0		ns	11
Output Buffer Turn-of	f Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
Transition Time (Rise	and Fall)	tт	3	50	3	50	3	50	ns	
RAS Precharge Time		tap	40		50		60		ns	
RAS Pulse Width		tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fas	t Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time		trsh	20		20		20		ns	
CAS Pulse Width		tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	·····	tcsн	60		70		80		ns	
RAS to CAS Delay Tir	ne	trco	20	40	20	50	25	60	ns	10
CAS to RAS Precharg	e Time	tcrp	10		10		10		ns	13
CAS Precharge Time		tcpn	10		10		10		ns	
CAS Precharge Time	(Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS H	lold Time	trpc	10		10		10		ns	
RAS Hold Time from	CAS Precharge	TRHCP	35		40		45		ns	
Row Address Setup T	ime	tasr	0		0		0		ns	
Row Address Hold Ti	me	trah	10.		10		12		ns	
Column Address Setu	p Time	tasc	0		0		0		ns	
Column Address Hold	l Time	tcah	15		15		15		ns	
Column Address Lead	Time Referenced to RAS	TRAL	30		35		40		ns	
Read Command Setu	p Time	trcs	0		0		. 0		ns	
Read Command Hold	Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold	Time Referenced to CAS	tясн	0		0		0		ns	14
WE Hold Time Refere	nced to CAS	twc _H	15		15		15		ns	15
Data-in Setup Time		tos	0		0		0		ns	16
Data-in Hold Time		tон	15		15		15		ns	16
Write Command Setup Time		twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)		tcsr	10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)		tchr	10		10		10		ns	
WE Setup Time		twsn	10		10		10		ns	
WE Hold Time		twnr	15		15		15		ns	
Refresh Time	Distributed refresh	tref		32		32		32	ms	
	Burst refresh			-16		16		16	ms	



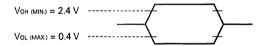
Notes

- 1. All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight CAS before RAS or RAS only
 refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (MAX.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart

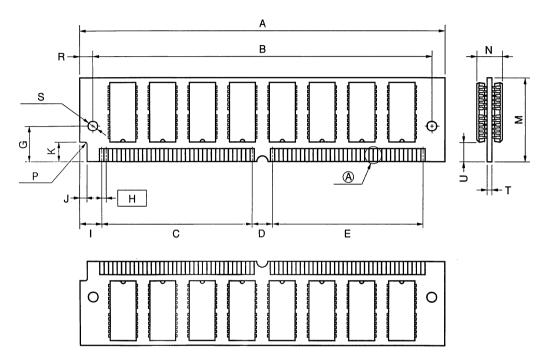
Please refer to Timing Chart 2, page 375.

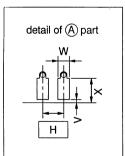


Package Drawings

[MC-428000A32B, 428000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



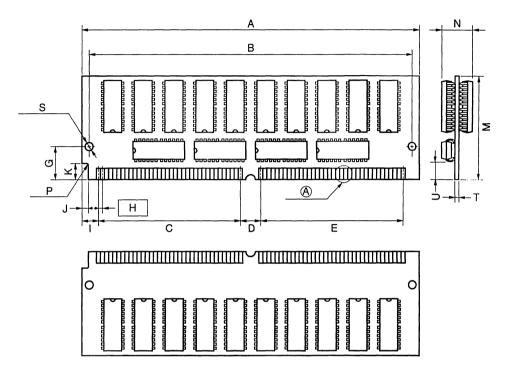


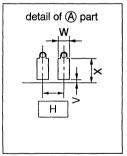
ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19±0.13	3.984 ^{+0.005} _{-0.006}
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
- 1	6.35	0.250
J	2.03	0.080
K	6.35	0.250
,M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Р	R1.57	R0.062
R	3.38±0.13	0.133+0.006
S	φ3.18	φ0.125
Т	1.27 +0.1 -0.08	0.050±0.004
U	5.5 MIN.	0.216 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55

[MC-428000A36BJ, 428000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
- 1	6.35	0.250
J	2.03	0.080
К	6.35	0.250
M	31.75	1.250
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
Т	1.27 ^{+0.1} -0.08	0.050±0.004
U	3.17 MIN.	0.124 MIN.
ν	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A50

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4 Byte SIMM [Hyper Page (EDO)]



CMOS INTEGRATED CIRCUIT

MC-421000F32

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-421000F32 is a 1,048,576 words by 32 bits dynamic RAM module on which 2 pieces of 16M DRAM: μ PD4218165 are assembled.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time	R/W cycle time	Hyper page mode	Power co (MAX.)	nsumption
(MAX.) (MIN.)	cycle time (MIN.)	Active	Standby		
MC-421000F32-60	60 ns	104 ns	25 ns	1,760 mW	11 mW
MC-421000F32-70	70 ns	124 ns	30 ns	1,650 mW	(CMOS level input)

- o 1,024 refresh cycle / 16ms
- o CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.



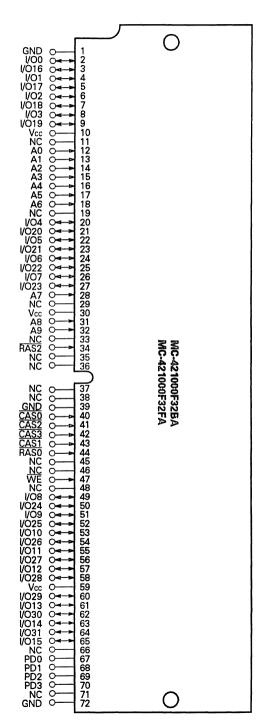
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000F32BA-60 MC-421000F32BA-70	60 ns 70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating(HAL)	2 pieces of μ PD4218165LE
MC-421000F32FA-60 MC-421000F32FA-70	60 ns 70 ns	72-pin Single In-line Memory Module (Socket Type)	(400mil SOJ) [Single side]



Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder coating, Gold plating)



A0-A9 : Address Inputs
I/O0-I/O31 : Data Inputs/Outputs
CAS0-CAS3 : Column Address Strobe
RAS0,RAS2 : Row Address Strobe
WE : Write Enable

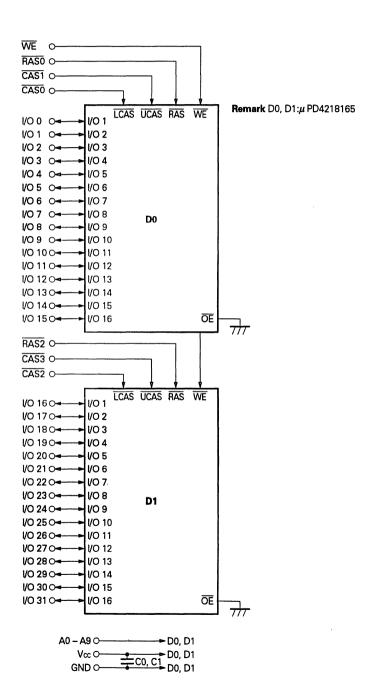
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin	Pin	Acces	s Time
Name	No.	60ns	70ns
PD0	67	GND	GND
PD1	68	GND	GND
PD2	69	NC	GND
PD3	70	NC	NC



Block Diagram





Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply Voltage	Vcc		-1.0 to +7.0	V
Output Current	lo		50	mA
Power Dissipation	Po		2	w
Operating Ambient Temperature	TA		0 to +70	°C
Storage Temperature	Tatg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	Vcc		4.5	5.0	5 .5	٧
High Level Input Voltage	ViH		2.4		Vcc +1.0	٧
Low Level Input Voltage	VIL		-1.0		+0.8	V
Operating Ambient Temperature	TA		0		70	°C

Capacitance (Ta = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	Cıı	A0 - A9			30	pF
	Cı2	WE			34	
	Сіз	RASO, RAS2			22	
	C14	CAS0 - CAS3			22	
Data Input/Output Capacitance	Cyo	I/O0 - I/O31			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc(MIN.)	trac = 60 ns		320	mA	1,2,3
		lo = 0 mA	trac = 70 ns		300		,,,,
Standby current	RAS, CAS ≧ VIH (MIN.), Io = 0 mA		\		4	mA	
Standby current	1002	RAS, CAS ≥ Vcc - 0.2 V, lo = 0 r	mA		2	mA	
===		RAS Cycling CAS ≧ Viн (MIN.)	trac = 60 ns		320	mA	1,2,3,4
RAS only refresh current	Iccs	trc = trc (MIN.) lo = 0 mA	trac = 70 ns		300		1,2,0,4
Operating current	Icc4	RAS ≦ VIL (MAX.) CAS Cycling	trac = 60 ns		220	mA	1,2,5
(Hyper page mode)	1004	thpc = thpc (MIN.) lo = 0 mA	trac = 70 ns		200		
CAS before RAS	lcc5	RAS Cycling tnc = tnc (MIN.)	trac = 60 ns		320	mA	1,2
Tonesh durient		lo = 0 mA	trac = 70 ns		300		
Input leakage current	li (L)	V _I = 0 to 5.5 V all other pins not under test = 0 V		-10	+10	μА	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μА	
High level output voltageLow	Vон	lo = -2.5 mA		2.4		٧	
level output voltage	Vol	lo = +2.1 mA			0.4	٧	

Notes 1. Icc1, Icc3, Icc4, Icc5 depend on cycle rates (tRc and tHPC).

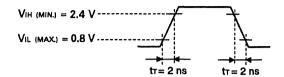
- 2. Specified values are obtained with outputs unloaded.
- 3. Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL(MAX.) and CAS ≥ VIH(MIN.).
- 4. Iccs is measured assuming that all column address inputs are held at either high or low.
- 5. Icc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.



AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification

(3) Loading conditions are 100 pF + 1 TTLs.

Common to Read, Write Cycle

Parameter	Symbol	trac =	60 ns	trac = 70 ns		115:4	Notes
rarameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	trc	104	_	124	_	ns	
RAS Precharge Time	trp	40	_	50	_	ns	
CAS Precharge Time	tcpn	10	_	10		ns	
RAS Pulse Width	tras	60	10 000	70	10 000	ns	
CAS Pulse Width	tcas	10	10 000	12	10 000	ns	
RAS Hold Time	tязн	10	_	12	_	ns	
CAS Hold Time	tсsн	40	_	50		ns	
RAS to CAS Delay Time	trco	14	45	14	52	ns	1
RAS to Column Address Delay Time	trad	12	30	12	35	ns	1
CAS to RAS Precharge Time	tcrp	5	_	5	_	ns	2
Row Address Setup Time	tasr	0	_	0	_	ns	
Row Address Hold Time	tŗан	10	_	10	_	กร	
Column Address Setup Time	tasc	0	_	0	-	กร	
Column Address Hold Time	tcah	10	_	12		ns	
CAS to Data Setup Time	tcız	0	_	0	_	ns	
Transition Time (Rise and Fall)	tт	1	50	1	50	ns	
Refresh Time	tref	_	16		16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	trac (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

tradimax.) and tradimax.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or taxc) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ tradimax.) and trad ≥ tradimax.) will not cause any operation problems.

2. tcrp(MIN.) requirement is applied to RAS, CAS cycles.

Read Cycle

Parameter	Sumb al	trac = 60 ns		trac = 70 ns		Unit	Notes
rarameter	Symbol	MIN.	MAX.	MIN.	MAX.	Onit	Notes
Access Time from RAS	trac	_	60	_	70	ns	1
Access Time from CAS	tcac	_	15	_	18	ns	1
Access Time from Column Address	taa	_	30	_	35	ns	1
Column Address Lead Time Referenced to RAS	tral	30	_	35	_	ns	
Read Command Setup Time	trcs	0		0	_	ns	
Read Command Hold Time Referenced to RAS	trrh	0		0	_	ns	2
Read Command Hold Time Referenced to CAS	trch	0	_	0	_	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≦ trad (MAX.) and trcd ≦ trcd (MAX.)	TRAC (MAX.)	trac (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

tradimax.) and tradimax.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ tradimax.) and trad ≥ tradimax.) will not cause any operation problems.

2. Either trch(MIN.) or trrh(MIN.) should be met in read cycles.



Write Cycle

D	Symbol	trac = 60 ns		trac = 70 ns			
Parameter		MIN.	MAX.	MIN.	MAX.	Unit	Notes
WE Hold Time Referenced to CAS	twcн	10	-	10	_	ns	
WE Setup Time	twcs	0		0	_	ns	1
Data-in Setup Time	tos	0	_	0	_	ns	2
Data-in Hold Time	t DH	10	_	10	_	ns	2

- Notes 1. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 - 2. tosimin.) and tohimin.) are referenced to the CAS falling edge in early write cycles.



Hyper Page Mode

_		trac = 60 ns		trac = 70 ns		l Imia	
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	tHPC	25	_	30	_	ns	1
RAS Pulse Width	trasp	60	125 000	70	125000	ns	
CAS Pulse Width	thcas	10	10 000	12	10 000	ns	
CAS Precharge Time	tcp	10	_	10	_	ns	
Access Time from CAS Precharge	tacp	_	35	_	40	ns	
RAS Hold Time from CAS Precharge	trhcp	35	_	40	_	ns	
Data Output Hold Time	tонс	5	_	5	_	ns	
Output Buffer Turn-off Delay from WE	twez	0	13	0	15	ns	2,3
WE Pulse Width	twpz	10	-	10	_	ns	3
Output Buffer Turn-off Delay from RAS	tofr	0	13	0	15	ns	2.3
Output Buffer Turn-off Delay from CAS	torc	0	13	0	15	ns	2.3

Notes 1. thec(MIN.) is applied to access time from CAS

- 2. tofc(MAX), tofr(MAX) and twez(MAX) define the time when the output achieves the condition of Hi-Z and is not referenced to VoH or VoL.
- 3. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE as follows. The effective specification depends on state of each signal.
 - (1) Both RAS and CAS are Inactive (at the end of read cycle)

WE : inactive

torc is effective when RAS is inactivated before CAS is inactivated.

toff is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are inactive or RAS is active and CAS is inactive(at the end of read cycle)
WE: active and either trank or track must be met... twez and twez is effective.

Refresh Cycle

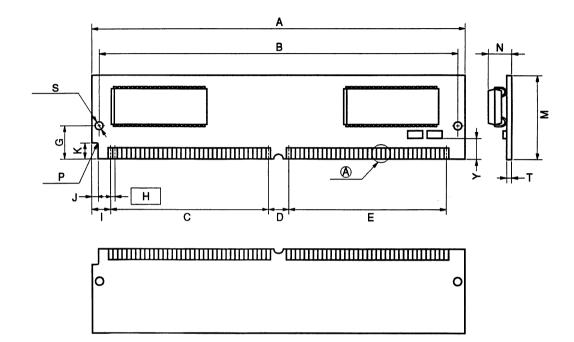
	Symbol		trac = 60 ns		trac = 70 ns		
Parameter			MAX.	MIN.	MAX.	Unit	Note
CAS Setup Time	tcsr	5	_	5	_	ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10	_	10	_	ns	
RAS Precharge CAS Hold Time	tRPC	5		5		ns	
WE Hold Time (Hidden Refresh Cycle)	twhr	15		15		ns	

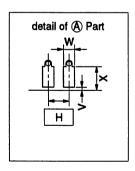
Timing Chart

Please refer to Timing Chart 3, page 385.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
1	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
Р	R1.57	R0.062
S	φ3.18	φ0.125
Τ	1.27 ^{+0.1} -0.08	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Υ	3.17 MIN.	0.124 MIN.
		14707 50440

M72B-50A46



CMOS INTEGRATED CIRCUIT

MC-422000F32

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-422000F32 is a 2,097,152 words by 32 bits dynamic RAM module on which 4 pieces of 16M DRAM: μPD4218165 are assembled.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- o 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time	R/W cycle time	Hyper page mode	Power co (MA	nsumption X.)	
(MAX.)		(MIN.) cycle time (MIN.)		Active	Standby	
MC-422000F32-60	60 ns	104 ns	25 ns	1,782 mW	22 mW	
MC-422000F32-70	70 ns	124 ns	30 ns	1,122 mW	(CMOS level input)	

- o 1,024 refresh cycle / 16ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.



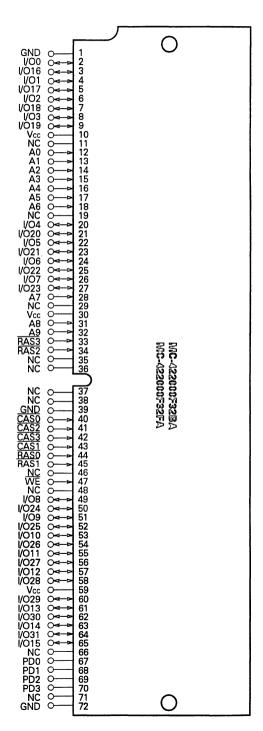
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000F32BA-60 MC-422000F32BA-70	60 ns 70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating(HAL)	4 pieces of μ PD4218165LE
MC-422000F32FA-60 MC-422000F32FA-70	60 ns 70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	(400mil SOJ) [Single side]

NEC

Pin Configuration

72-pin Single In-line Momory Modulo Socket Typo (Edgo connector : Solder coating, Gold plating)



A0-A9 : Address Inputs 1/00-1/031 : Data Inputs/Outputs CASO-CAS3 : Column Address Strobe RAS0-RAS3 : Row Address Strobe

WE

: Write Enable

Vcc

: Power Supply

GND

: Ground

: No connection

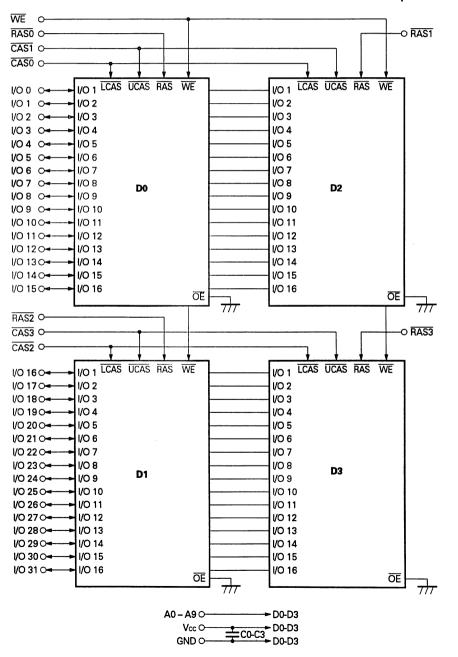
The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin	Pin	Access Time		
Namo	No.	60ns	70ns	
PD0	67	NC	NC	
PD1	68	NC	NC	
PD2	69	NC	GND	
PD3	70	NC	NC	



Block Diagram

Remark D0-D3 : μPD4218165





Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	٧
Supply Voltage	Vcc		-1.0 to +7.0	v
Output Current	lo		50	mA
Power Dissipation	Po		4	w
Operating Ambient Temperature	TA		0 to +70	°C
Storage Temperature	Tatg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	Vcc		4.5	5.0	5.5	٧
High Level Input Voltage	Vıн		2.4		Vcc +1.0	V
Low Level Input Voltage	VIL		-1.0		+0.8	٧
Operating Ambient Temperature	TA		0		70	°C

Capacitance (Ta = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Uniț
Input Capacitance	Ci1	A0 - A9			40	pF
	C ₁₂	WE			48	
	Сіз	RASO - RAS3	l'		22	
	C ₁₄	CASO - CAS3			29	
Data Input/Output Capacitance	Cyo	I/O0 - I/O31			26	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc(MIN.)	trac = 60 ns		324	mA	1,2,3
		lo = 0 mA	trac = 70 ns		304		
Standby current	lcc2	RAS, CAS ≥ VIH (MIN.), Io = 0 mA	TAS, CAS ≧ VIH (MIN.), Io = 0 mA		8		
Standby current	1002	RAS, CAS ≥ Vcc - 0.2 V, lo = 0 r	mA		4	mA	·
	RAS Cycling CAS ≥ ViH (MIN.) TRAC = 60 ns		trac = 60 ns		324	mA	1,2,3,4
RAS only refresh current	lcc3	trc = trc (MIN.) lo = 0 mA	trac = 70 ns		304		1,2,0,1
Operating current	Icc4	RAS ≦ VIL (MAX.) CAS Cycling	trac = 60 ns		224	mA	1,2,5
(Hyper page mode)	1004	thpc = thpc (MIN.) lo = 0 mA	trac = 70 ns		204		
CAS before RAS	lcc5	RAS Cycling trc = trc (MIN.)	trac = 60 ns		324	mA	1,2
Tellesii cultelit		lo = 0 mA	lo = 0 mA trac = 70 ns		304		
Input leakage current	lı (L)	V _I = 0 to 5.5 V all other pins not under test = 0	-10	+10	μА		
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μΑ		
High level output voltageLow	Vон	lo = -2.5 mA	2.4		٧		
level output voltage	Vol	lo = +2.1 mA		0.4	٧		

Notes 1. Icc1, Icc3, Icc4, Icc5 depend on cycle rates (trc and thrc).

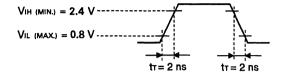
- 2. Specified values are obtained with outputs unloaded.
- 3. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{RAS} \le V_{IL(MAX.)}$ and $\overline{CAS} \ge V_{IH(MIN.)}$.
- 4. Iccs is measured assuming that all column address inputs are held at either high or low.
- lcc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.



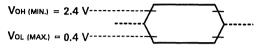
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTLs.

Common to Read, Write Cycle

P	0	trac =	trac = 60 ns		trac = 70 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	trc	104	_	124		ns	
RAS Precharge Time	trp	40	_	50	_	ns	
CAS Precharge Time	tcpn	10	_	10		ns	
RAS Pulse Width	tras	60	10 000	70	10 000	ns	
CAS Pulse Width	tcas	10	10 000	12	10 000	ns	
RAS Hold Time	trsh	10	_	12	_	ns	
CAS Hold Time	tсsн	40		50	_	ทธ	
RAS to CAS Delay Time	trcD	14	45	14	52	ns	1
RAS to Column Address Delay Time	trad	12	30	12	35	ns	1
CAS to RAS Precharge Time	tcrp	5	_	5	_	ns	2
Row Address Setup Time	tasr	0	_	0	_	ns	
Row Address Hold Time	trah	10	_	10		ns	
Column Address Setup Time	tasc	0	_	0	_	ns	
Column Address Hold Time	tcah	10	_	12	_	ทธ	
CAS to Data Setup Time	tcLZ	0	_	0	_	ns	
Transition Time (Rise and Fall)	tτ	1	50	1	50	ns	
Refresh Time	tref	_	16	_	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS	
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	trac (MAX.)	
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)	
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)	

tradimax.) and tradimax.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ tradimax.) and trade tradimax.) will not cause any operation problems.

2. tcrp(MIN.) requirement is applied to RAS, CAS cycles.

Read Cycle

Parameter	Symbol	trac = 60 ns		trac = 70 ns		Unit	Notes
Farameter		MIN.	MAX.	MIN.	MAX.	Oiiit	Notes
Access Time from RAS	trac	_	60	_	70	ns	1
Access Time from CAS	tcac		15	_	18	ns	1
Access Time from Column Address	taa	[-	30		35	ns	1
Column Address Lead Time Referenced to RAS	tral	30	_	35	_	ns	
Read Command Setup Time	trcs	0	_	0	_	ns	
Read Command Hold Time Referenced to RAS	trrh	0	_	0	_	ns	2
Read Command Hold Time Referenced to CAS	tпсн	0	_	0	_	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	trac (MAX.)	trac (max.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (MAX.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad(MAX.) and trad(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad(MAX.) and tracd ≥ trad(MAX.) will not cause any operation problems.

2. Either trch(MIN.) or trrh(MIN.) should be met in read cycles.



Write Cycle

Parameter	Symbol	trac = 60 ns		trac = 70 ns			
		MIN.	MAX.	MIN.	MAX.	Unit	Notes
WE Hold Time Referenced to CAS	twcн	10	_	10	_	ns	
WE Setup Time	twcs	0	_	0	_	ns	1
Data-in Setup Time	tos	0		0	_	ns	2
Data-in Hold Time	tон	10	_	10	_	ns	2

- Notes 1. If twcs ≧ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 - 2. tos(MIN.) and toh(MIN.) are referenced to the CAS falling edge in early write cycles.



Hyper Page Mode

Symbol	trac = 60 ns		trac = 70 ns			
	MIN.	MAX.	MIN.	MAX.	. Unit N	Notes
thpc	25	_	30	_	ns	1
trasp	60	125 000	70	125000	ns	
thcas	10	10 000	12	10 000	ns	
tcp	10	_	10	_	ns	
tacp	_	35	_	40	ns	
trhcp	35	-	40	_	ns	
tонс	5	_	5	_	ns	
twez	0	13	0	15	ns	2,3
twpz	10	_	10	_	ns	3
tofr	0	13	0	15	ns	2.3
torç	0	13	0	15	ns	2.3
	thpc trasp thcas tcp tacp trhce tohc twez twpz tofr	Symbol MIN.	Symbol MIN. MAX. thpc 25 — trasp 60 125 000 thcas 10 10 000 tcp 10 — tacp — 35 trhcp 35 — tdhc 5 — twez 0 13 twpz 10 — tofr 0 13	Symbol MIN. MAX. MIN. thpc 25 — 30 trasp 60 125 000 70 thcas 10 10 000 12 tcp 10 — 10 tacp — 35 — trhcp 35 — 40 tohc 5 — 5 twez 0 13 0 twpz 10 — 10 tofr 0 13 0	Symbol MIN. MAX. MIN. MAX. thpc 25 — 30 — trasp 60 125 000 70 125000 thcas 10 10 000 12 10 000 tcp 10 — 10 — tacp — 35 — 40 — tracp 35 — 40 — — tbhc 5 — 5 — — twez 0 13 0 15 twpz 10 — 10 — tofr 0 13 0 15	Symbol MIN. MAX. MIN. MAX. Unit thr 25 — 30 — ns trasp 60 125 000 70 125000 ns thcas 10 10 000 12 10 000 ns tcp 10 — 10 — ns tACP — 35 — 40 ns tRHCP 35 — 40 — ns tDHC 5 — 5 — ns twez 0 13 0 15 ns tofr 0 13 0 15 ns

Notes 1. thec(MIN.) is applied to access time from CAS

- 2. tofc(MAX.), tofr(MAX.) and twez(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to VoH or VoL.
- 3. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE as follows. The offective specification depends on state of each signal.
 - (1) Both RAS and CAS are Inactive (at the end of read cycle)

WE: inactive

torc is effective when $\overline{\rm RAS}$ is inactivated before $\overline{\rm CAS}$ is inactivated.

tofR is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are inactive or RAS is active and CAS is inactive(at the end of read cycle)
WE: active and either trank or track must be met... twez and twez is effective.

Refresh Cycle

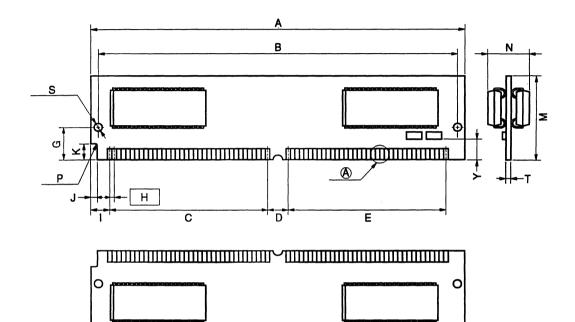
		trac =	: 60 ns	trac = 70 ns			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Note
CAS Setup Time	tcsR	5		5	_	ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10	_	ns	
RAS Precharge CAS Hold Time	trpc	5	_	5	_	ns	
WE Hold Time (Hidden Refresh Cycle)	twnr	15	_	15	_	ns	

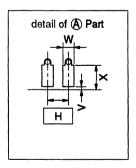
Timing Chart

Please refer to Timing Chart 3, page 385.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19	3.984
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
1	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Р	R1.57	R0.062
S	φ3.18	φ0.125
Т	1.27 ^{+0.1} -0.08	0.050±0.004
٧	0.25 MAX.	0.010 MAX.
w	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.
•		M72D-E0 A45



CMOS INTEGRATED CIRCUIT

MC-424000F32

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-424000F32 is a 4,194,304 words by 32 bits dynamic RAM module on which 8 pieces of 16M DRAM: μPD4217405 are assembled.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time	R/W cycle time	Hyper page mode	Power o (MAX.)	onsumption
1 anniy	(MAX.)	(MIN.)	cycle time (MIN.)	Active	Standby
MC-424000F32-60	60 ns	104 ns	25 ns	4,840 mW	44 mW
MC-424000F32-70	70 ns	124 ns	30 ns	4,400 mW	(CMOS level input)

- 2,048 refresh cycle / 32ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.

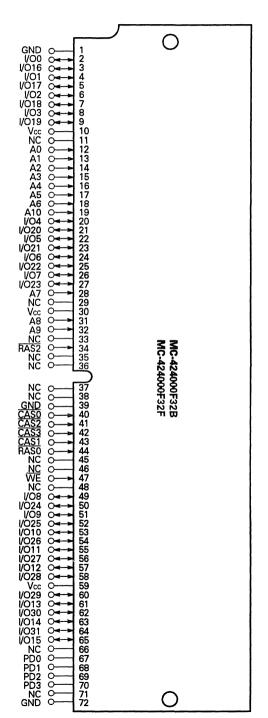


Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000F32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type)	8 pieces of μ PD4217405LA
MC-424000F32B-70	70 ns	Edge connector: Solder coating(HAL)	(300mil SOJ)
MC-424000F32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type)	•
MC-424000F32F-70	70 ns	Edge connector: Gold plating	[Single side]

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder coating, Gold plating)



A0-A10 : Address Inputs

I/O0-I/O31 : Data Inputs/Outputs

CAS0-CAS3 : Column Address Strobe

RAS0.RAS2 : Row Address Strobe

WE : Write Enable

Vcc : Power Supply

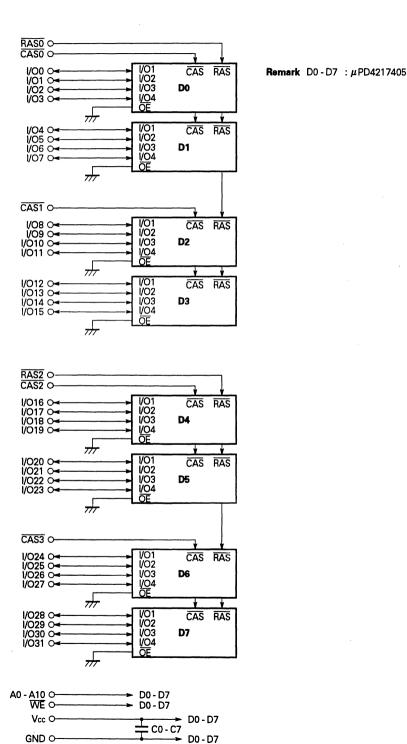
GND : Ground

NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin	Pin	Access Time			
Name	No.	60ns	70ns		
PD0	67	GND	GND		
PD1	68	NC	NC		
PD2	69	NC	GND		
PD3	70	NC	NC		

Block Diagram





Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply Voltage	Vcc		-1.0 to +7.0	٧
Output Current	lo		50	mA
Power Dissipation	Po		8	w
Operating Ambient Temperature	TA		0 to +70	°C
Storage Temperature	Tatg		-55 to +125	•€

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	Vcc		4.5	5.0	5.5	٧
High Level Input Voltage	ViH		2.4		Vcc +1.0	٧
Low Level Input Voltage	VIL		-1.0		+0.8	٧
Operating Ambient Temperature	TA		0		70	°C

Capacitance (Ta = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	Cıı	A0 - A10			68	pF
	C ₁₂	WE			76	
	Сіз	RASO, RAS2			43	
	C ₁₄	CAS0 - CAS3			29	
Data Input/Output Capacitance	Ci/o	I/O0 - I/O31			17	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc(MIN.)	trac = 60 ns		880	mA	1,2,3
		lo = 0 mA	trac = 70 ns		800		
Standby current	lcc2	RAS, CAS ≥ Vih (MIN.), Io = 0 mA			16		
Standby current	ICC2	RAS, CAS ≧ Vcc - 0.2 V, lo = 0 r	mA		8	mA .	
		RAS Cycling CAS ≧ Vih (MIN.)	trac = 60 ns		880	mA	1,2,3,4
RAS only refresh current	Icc3	trc = trc (MIN.) lo = 0 mA	trac = 70 ns		800		,_,_,
Operating current	lcc4	RAS ≦ VIL (MAX.) CAS Cycling	trac = 60 ns		720	mA	1,2,5
(Hyper page mode)	1004	thpc = thpc (MIN.) lo = 0 mA	trac = 70 ns		640		
CAS before RAS	Іссь	RAS Cycling trc = trc (MIN.)	trac = 60 ns		880	mA	1,2
Tonesir durient		lo = 0 mA	trac = 70 ns		800		
Input leakage current	li (L)	V _I = 0 to 5.5 V all other pins not under test = 0 V		-10	+10	μА	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μΑ	
High level output voltageLow	Vон	lo = -2.5 mA		2.4		٧	
level output voltage	Vol	lo = +2.1 mA			0.4	٧	

Notes 1. Icc1, Icc3, Icc4, Icc5 depend on cycle rates (trc and thrc).

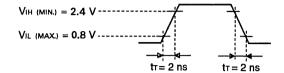
- 2. Specified values are obtained with outputs unloaded.
- 3. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{RAS} \le V_{IL(MAX.)}$ and $\overline{CAS} \ge V_{IH(MIN.)}$.
- 4. Iccs is measured assuming that all column address inputs are held at either high or low.
- 5. Icc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.



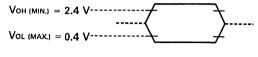
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write Cycle

Parameter		trac =	60 ns	trac = 70 ns]
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	t RÇ	104		124	_	ns	
RAS Precharge Time	trp	40	-	50	_	ns	
CAS Precharge Time	tcpn	10	_	10	_	ns	
RAS Pulse Width	tras	60	10 000	70	10 000	ns	
CAS Pulse Width	tcas	10	10 000	12	10 000	ns	
RAS Hold Time	tпsн	10	_	12	_	ns	
CAS Hold Time	tсsн	40	_	50	_	ns	
RAS to CAS Delay Time	trcd	14	45	14	52	ns	1
RAS to Column Address Delay Time	trad	12	30	12	35	ทธ	1
CAS to RAS Precharge Time	tcrp	5	_	5	_	ทธ	2
Row Address Setup Time	tasr	0	_	0	_	ทธ	
Row Address Hold Time	trah	10	_	10	_	ns	
Column Address Setup Time	tasc	0		0	_	ns	
Column Address Hold Time	tcah	10	_	12		ns	
CAS to Data Setup Time	tcLZ	0		0	_	ns	
Transition Time (Rise and Fall)	tτ	1	50	1	50	ns	
Refresh Time	tref	_	16	_	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	trac (MAX.)	trac (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad(MAX.) and trad(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or taxc) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad(MAX.) and trad ≥ trad(MAX.) will not cause any operation problems.

2. tcrp(MIN.) requirement is applied to RAS, CAS cycles.

Read Cycle

Parameter	Symbol	trac = 60 ns		trac = 70 ns		Unit	Notes
rarameter		MIN.	MAX.	MIN.	MAX.	Oill	Notes
Access Time from RAS	trac	_	60	_	70	ns	1
Access Time from CAS	tcac	_	15		18	ns	1
Access Time from Column Address	taa		30		35	ns	1
Column Address Lead Time Referenced to RAS	tral	30	_	35	_	ns	
Read Command Setup Time	trcs	0	_	0	_	ns	
Read Command Hold Time Referenced to RAS	trrh	0	_	0	_	ns	2
Read Command Hold Time Referenced to CAS	tпсн	0	_	0		ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (MAX.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (max.)

trad(MAX.) and trad(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad(MAX.) and trad ≥ trad(MAX.) will not cause any operation problems.

2. Either trch(MIN.) or trrh(MIN.) should be met in read cycles.



Write Cycle

Parameter		trac = 60 ns		trac = 70 ns			
	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
WE Hold Time Referenced to CAS	twcн	10		10	_	ns	
WE Setup Time	twcs	0	_	0	_	ns	1
Data-in Setup Time	tos	0	_	0	_	ns	2
Data-in Hold Time	tон	10	_	10	-	ns	2

Notes 1. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

2. tds(MIN.) and tdH(MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.



Hyper Page Mode

		trac = 60 ns		trac = 70 ns			
Parameter	Parameter Symbol		MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	thec	25	_	30	_	ns	1
RAS Pulse Width	trasp	60	125 000	70	125000	ns	
CAS Pulse Width	thcas	10	10 000	12	10 000	ns	
CAS Precharge Time	tcp	10	-	10	_	ns	
Access Time from CAS Precharge	tacp	_	35	_	40	ns	
RAS Hold Time from CAS Precharge	trhcp	35	_	40	_	ns	
Data Output Hold Time	tonc	5	_	5	_	ns	
Output Buffer Turn-off Delay from WE	twez	0	13	0	15	ns	2,3
WE Pulse Width	twpz	10	_	10	-	ns	3
Output Buffer Turn-off Delay from RAS	tofr	0	13	0	15	ns	2.3
Output Buffer Turn-off Delay from CAS	torc	0	13	0	15	ns	2.3

Notes 1. thrc(MIN.) is applied to access time from CAS

- 2. torc(MAX.), torr(MAX.) and twez(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to VoH or VoL.
- 3. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE as follows. The effective specification depends on state of each signal.
 - (1) Both RAS and CAS are Inactive (at the end of read cycle)

WE: inactive

torc is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

toff is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are inactive or RAS is active and CAS is inactive(at the end of read cycle)

WE: active and either trank or track must be met... twez and twez is effective.

Refresh Cycle

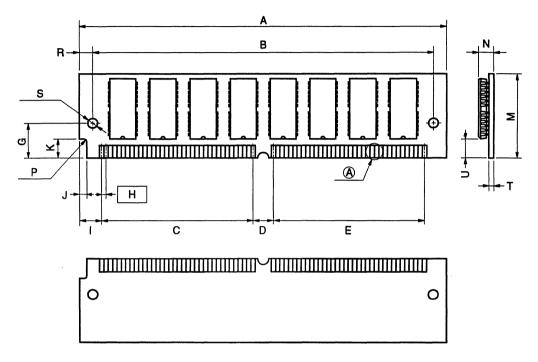
		trac = 60 ns		trac = 70 ns			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Note
CAS Setup Time	tcsa	5		5	_	ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10	_	10	_	ns	
RAS Precharge CAS Hold Time	tapc	5	_	5	_	ns	
WE Hold Time	twnr	15	_	15	_	ns	
WE Setup Time	twsn	10		10	_	กร	

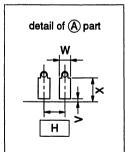
Timing Chart

Please refer to Timing Chart 4, page 397.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19±0.13	3.984 ^{+0.005} _{-0.006}
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
!	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
N	5.08 MAX.	0.200 MAX.
Р	R1.57	R0.062
R	3.38±0.13	0.133 + 0.006 -0.005
S	φ3.18	φ0.125
Т	1.27 ±0.1 -0.08	0.050±0.004
U	5.5 MIN.	0.216 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
		1470D 50454

M72B-50A54



CMOS INTEGRATED CIRCUIT

MC-428000F32

8 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-428000F32 is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16M DRAM: μPD4217405 are assembled.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- o 8,388,608 words by 32 bits organization
- Fast access and cycle time

Family	Access time	R/W cycle time	Hyper page mode	Power co (MAX.)	ensumption
1 dillily	(MAX.)	(MIN.)	cycle time (MIN.)	Active	Standby
MC-428000F32-60	60 ns	104 ns	25 ns	5,170 mW	88 mW
MC-428000F32-70	70 ns	124 ns	30 ns	4,730 mW	(CMOS level input)

- o 2,048 refresh cycle / 32ms
- o CAS before RAS refresh, RAS only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

The information in this document is subject to change without notice.



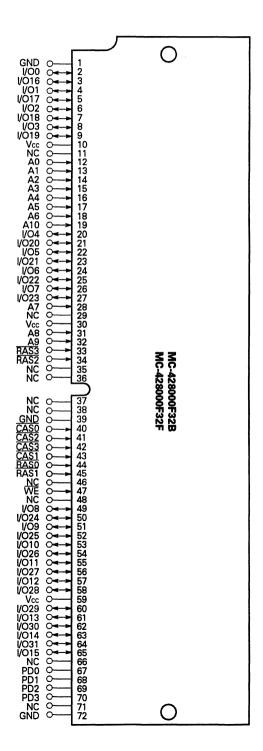
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000F32B-60 MC-428000F32B-70	60 ns 70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating(HAL)	16 pieces of μ PD4217405LA
MC-428000F32F-60 MC-428000F32F-70	60 ns 70 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	(300mil SOJ) [Single side]



Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder coating, Gold plating)



A0-A10 : Address Inputs

I/O0-I/O31 : Data Inputs/Outputs

CAS0-CAS3 : Column Address Strobe

RAS0-RAS3 : Row Address Strobe

WE : Write Enable

Vcc : Power Supply

GND : Ground

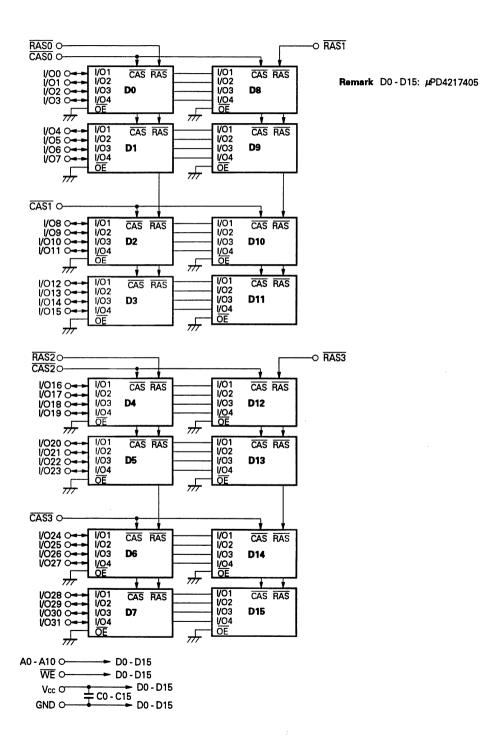
NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin	Pin	Acces	s Time
Name	No.	60ns	70ns
PD0	67	NC	NC
PD1	68	GND	GND
PD2	69	NC	GND
PD3	70	NC	NC



Block Diagram





Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply Voltage	Vcc		-1.0 to +7.0	V
Output Current	lo		50	mA
Power Dissipation	Po		16	w
Operating Ambient Temperature	TA		0 to +70	°C
Storage Temperature	Tatg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	Vcc		4.5	5.0	5.5	٧
High Level Input Voltage	ViH		2.4		Vcc +1.0	٧
Low Level Input Voltage	VIL		-1.0		+0.8	٧
Operating Ambient Temperature	TA		0		70	°C

Capacitance (Ta = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	Cıı	A0 - A10			121	pF
	C ₁₂	WE			137	
	Сіз	RASO - RAS3			48	
	C14	CASO - CAS3			48	
Data Input/Output Capacitance	Ci/o	I/O0 - I/O31			29	рF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling trc = trc(MIN.)	trac = 60 ns		940	mA	1,2,3
		lo = 0 mA	trac = 70 ns		860		,,_,,
Standby current	lcc2	RAS, CAS ≥ VIH (MIN.), Io = 0 mA	RAS, CAS ≧ VIH (MIN.), Io = 0 mA		32	mA	
Standby Surrent	1002	RAS, CAS ≧ Vcc - 0.2 V, lo = 0 r	πА		16	MA	
		RAS Cycling CAS ≧ VIH (MIN.)	trac = 60 ns		940	mA	1,2,3,4
RAS only refresh current	Іссз	trc = trc (MIN.) lo = 0 mA	trac = 70 ns		860	,	1,2,0,4
Operating current	Icc4	RAS ≦ VIL (MAX.) CAS Cycling	TRAC = 60 ns		780	mA	1,2,5
(Hyper page mode)	ICC4	thpc = thpc (MIN.) lo = 0 mA	trac = 70 ns		700		.,
CAS before RAS	Icc5	RAS Cycling trc = trc (MIN.)	trac = 60 ns		940	mA	1,2
Terresir current		lo = 0 mA	trac = 70 ns		860		.,_
Input leakage current	lı (L)	V _I = 0 to 5.5 V all other pins not under test = 0	-10	+10	μА		
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)	-10	+10	μА		
High level output voltageLow	Vон	lo = -2.5 mA	2.4		٧		
level output voltage	Vol	lo = +2.1 mA		0.4	٧		

Notes 1. Icc1, Icc3, Icc4, Icc5 depend on cycle rates (tRc and tHPC).

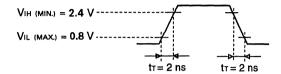
- 2. Specified values are obtained with outputs unloaded.
- 3. Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VILIMAX.) and CAS ≥ VIHIMIN.).
- 4. lcc3 is measured assuming that all column address inputs are held at either high or low.
- 5. lcc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.



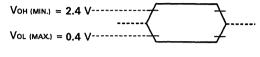
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write Cycle

P	G	trac = 60 ns		trac = 70 ns			Notes
Parameter	Symbol	MIN. MAX.		MIN. MAX.		Unit	
Read / Write Cycle Time	t RC	104	_	124	_	ns	
RAS Precharge Time	t RP	40	_	50	_	ns	
CAS Precharge Time	topn	10		10	_	ns	
RAS Pulse Width	tras	60	10 000	70	10 000	ns	
CAS Pulse Width	tcas	10	10 000	12	10 000	ns	
RAS Hold Time	tязн	10	_	12	_	ns	
CAS Hold Time	tсsн	40		50	_	ns	
RAS to CAS Delay Time	trcd	14	45	14	52	ns	1
RAS to Column Address Delay Time	trad	12	30	12	35	ns	1
CAS to RAS Precharge Time	tcrp	5	_	5	_	ns	2
Row Address Setup Time	tasr	0	_	0	_	ns	
Row Address Hold Time	trah	10	_	10	_	ns	
Column Address Setup Time	tasc	0	_	0	_	ns	
Column Address Hold Time	t cah	10	_	12		ns	
CAS to Data Setup Time	tcLz	0	_	0	_	ns	
Transition Time (Rise and Fall)	tτ	1	50	1	50	ns	
Refresh Time	tref		16	_	16	ms	



Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad(MAX.) and trad(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or taxc) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad(MAX.) and trad ≥ trad(MAX.) will not cause any operation problems.

2. tcrp(MIN.) requirement is applied to RAS, CAS cycles.

Read Cycle

Danier de la constante de la c	Cours has l	trac = 60 ns		trac = 70 ns		Unit	Notes
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Oint	Notes
Access Time from RAS	trac	_	60	_	70	ns	1
Access Time from CAS	tcac	_	15	-	18	ns	1
Access Time from Column Address	taa	_	30	1	35	ns	1
Column Address Lead Time Referenced to RAS	tral	30	_	35	_	ns	
Read Command Setup Time	trcs	0	_	0	-	ns	
Read Command Hold Time Referenced to RAS	trrh	0	_	0		ns	2
Read Command Hold Time Referenced to CAS	t RCH	0	_	0	_	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trod + tcac (max.)

trad(MAX.) and trcd(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad(MAX.) and trcd ≥ trcd(MAX.) will not cause any operation problems.

2. Either trch(MIN.) or trrh(MIN.) should be met in read cycles.



Write Cycle

Parameter	Symbol	trac = 60 ns		trac = 70 ns			
		MIN.	MAX.	MIN.	MAX.	Unit	Notes
WE Hold Time Referenced to CAS	twch	10	_	10	_	ns	
WE Setup Time	twcs	0	_	0	_	ns	1
Data-in Setup Time	tos	0	_	0	_	ns	2
Data-in Hold Time	t DH	10	_	10	_	ns	2

- Notes 1. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 - 2. tos(MIN.) and tDH(MIN.) are referenced to the CAS falling edge in early write cycles.



Hyper Page Mode

D		trac = 60 ns		trac = 70 ns		l	
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit N	Notes
Read / Write Cycle Time	thpc	25	_	30	_	ns	1
RAS Pulse Width	trasp	60	125 000	70	125000	ns	
CAS Pulse Width	thcas	10	10 000	12	10 000	ns	
CAS Precharge Time	tcp	10	_	10	_	ns	
Access Time from CAS Precharge	tacp	_	35		40	ns	
RAS Hold Time from CAS Precharge	trhcp	35	_	40	_	ns	
Data Output Hold Time	t DHC	5	_	5	_	ns	
Output Buffer Turn-off Delay from WE	twez	0	13	0	15	ns	2,3
WE Pulse Width	twpz	10	_	10	_	ns	3
Output Buffer Turn-off Delay from RAS	torr	0	13	0	15	ns	2.3
Output Buffer Turn-off Delay from CAS	torc	0	13	0	15	ns	2.3

Notes 1. thec(MIN.) is applied to access time from CAS

- 2. tofc(MAX.), tofr(MAX.) and twez(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to VoH or VoL.
- 3. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE as follows. The effective specification depends on state of each signal.
 - (1) Both RAS and CAS are Inactive (at the end of read cycle)

WE : inactive

torc is effective when RAS is inactivated before CAS is inactivated.

toff is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are inactive or RAS is active and CAS is inactive(at the end of read cycle)
WE : active and either tranh or trach must be met... twez and twez is effective.

Refresh Cycle

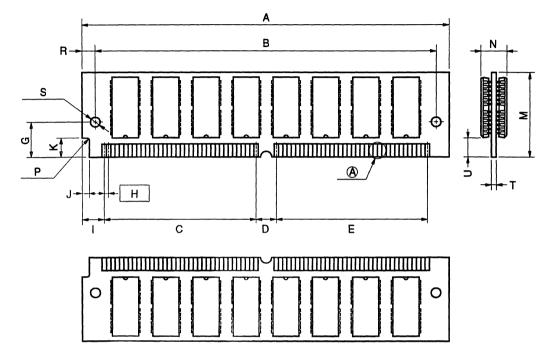
		trac = 60 ns		trac = 70 ns			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Note
CAS Setup Time	tcsR	5	_	5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10	_	ns	
RAS Precharge CAS Hold Time	trpc	5	_	5	_	ns	
WE Hold Time	twnr	15	_	15		ns	
WE Setup Time	twsR	10	_	10	_	ns	

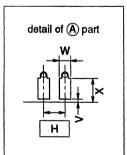
Timing Chart

Please refer to Timing Chart 4, page 397.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	107.95±0.13	4.250±0.006
В	101.19±0.13	3.984 ^{+0.005} _{-0.006}
С	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
Н	1.27 (T.P.)	0.050 (T.P.)
1	6.35	0.250
J	2.03	0.080
K	6.35	0.250
М	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Р	R1.57	R0.062
R	3.38±0.13	0.133 +0.006 -0.005
S	φ3.18	φ0.125
Т	1.27 ^{+0.1} -0.08	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55

Small Outline DIMM



MOS INTEGRATED CIRCUIT MC-42S1000LAD32S SERIES

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S1000LAD32S series is a 1,048,576 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 2 pieces of 16 M DRAM: μ PD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- CAS before RAS self refresh, CAS before RAS refresh, RAS only refresh, Hidden refresh
- 1,048,576 words by 32 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time	l.	onsumption IAX.)
(MAX.)	(IVIAX.)	(MIN.)	Active	Standby
MC-42S1000LAD32S-A60	60 ns	110 ns	1,080 mW	
MC-42S1000LAD32S-A70	70 ns	130 ns	1,008 mW	1.08 mW (CMOS level input)
MC-42S1000LAD32S-A80	80 ns	150 ns	936 mW	Civios level iliput/

- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

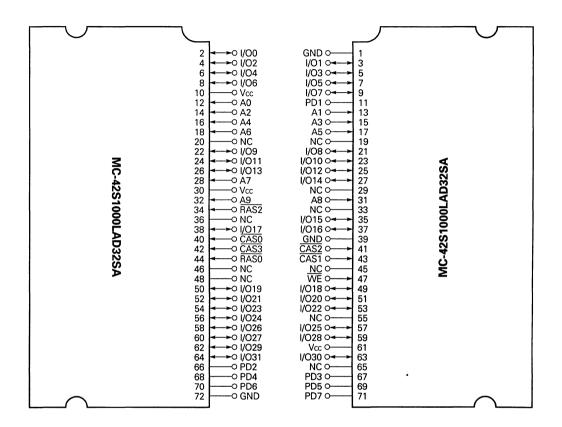


Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S1000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module	2 pieces of μPD42S18160LG5
MC-42S1000LAD32SA-A70	70 ns	(Socket Type)	(400 mil TSOP (II))
MC-42S1000LAD32SA-A80	80 ns	Edge connector: Gold plating	[Single side]

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



A0 - A9 I/O0 - I/O31 : Address Inputs

RASO, RAS2

: Data Inputs/Outputs: Row Address Strobe

CASO - CAS3

: Column Address Strobe

WE

: Write Enable

PD1 - PD7

: Presence Detect Pins

Vcc

: Power Supply

GND

: Ground

NC

: No connection

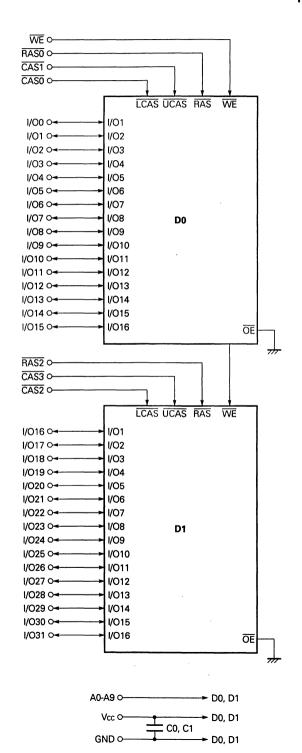
The internal connection of PD pins (PD1 to PD7).

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD1	11	NC	NC	NC		
PD2	66	GND	GND	GND		
PD3	67	GND	GND	GND		
PD4	68	NC	NC	NC		
PD5	69	NC	GND	NC		
PD6	70	NC	NC	GND		
PD7	71	GND	GND	GND		



Block Diagram

Remark D0, D1 : μPD42S18160L (TSOP (II))





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-0.5 to +4.6	٧
Supply voltage	Vcc		-0.5 to +4.6	٧
Output current	lo		20	mA
Power dissipation	Рь		2	w
Operating ambient temperature	TA		0 to +70	.c
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	٧
High level input voltage	ViH		2.0		Vcc + 0.3	٧
Low level input voltage	VIL		-0.3		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A9			29	
	C ₁₂	WE			29	_
	Сіз	RASO, RAS2			23	рF
	C14	CAS0 - CAS3			17	
Data Input/Output capacitance	Cvo	I/O0 - I/O31			12	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling	trac = 60 ns		300		
•		trc = trc (MIN.)	trac = 70 ns		280	mA	3, 4, 7
		lo = 0 mA	trac = 80 ns		260		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo ≈ 0 mA		1.0	1.0 mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		0.3		
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		300		
		CAS ≥ Vih (MIN.) trc = trc (MIN.)	trac = 70 ns		280	mA	3, 4, 5, 7
		lo = 0 mA	trac = 80 ns		260		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		180		
(Fast page mode)		tpc = tpc (MIN.)	trac = 70 ns		160	mA	3, 4, 6
		lo = 0 mA	trac = 80 ns		140		
CAS before RAS	Icc5	RAS Cycling	trac = 60 ns		300		
refresh current			trac = 70 ns		280	mA	3, 4
		lo = 0 mA	trac = 80 ns		260		
CAS before RAS long refresh current	Icce		tras ≤ 1 μs		360	μΑ	3, 4
CAS before RAS self refresh current	Icc7	$\overline{RAS}, \overline{CAS}:$ $trass = 5 ms$ $Vcc -0.2 \ V \le Vih \le Vih \ (MAX.)$ $0 \ V \le Vil \le 0.2 \ V$ $lo = 0 \ mA$			300	μΑ	4
Input leakage current	lı (L)	V _I = 0 to 3.6 V All other pins not under test = 0 V		-5	+5	μА	
Output leakage current	lo (L)	Vo = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μΑ	A delay a
High level output voltage	Vон	lo = -2.0 mA		2.4		٧	
Low level output voltage	Vol	lo = +2.0 mA			0.4	٧	



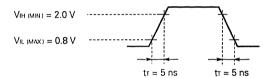
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

	<u> </u>	trac = 60 ns		trac = 70 ns		trac = 80 ns			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		15		20		20	ns	10, 11
Access Time Column Address	taa		30		35		40	ns	10, 11
Access Time from CAS Precharge	tace		35		40		45	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLZ	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	tт	3	50	3	50	3	50	ns	
RAS Precharge Time	tap	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	trsh	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcnp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	tRPC	5		5		5		ns	
RAS Hold Time from CAS Precharge	trhcp	35		40		45		ns	
Row Address Setup Time	tasr	0		0		0		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcan	15		15		15		ns	
Column Address Lead Time Referenced to RAS	TRAL	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
RAS Pulse Width (CAS before RAS Self Refresh)	trass	100		100		100		μs	
RAS Precharge Time (CAS before RAS Self Refresh)	trps	110		130		150		ns	
CAS Hold Time (CAS before RAS Self Refresh)	tcнs	-50		-50		-50		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	tref		128		128		128	ms	

Notes

- 1. All voltages are referenced to GND.
- 3. Icc1, Icc3, Icc4, Icc5 and Icc6 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t\tau = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification

10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and tred ≤ tred (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	TCAC (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

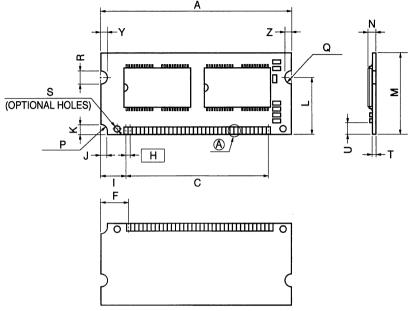
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trach (MIN.) or trach (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

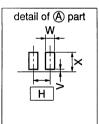
Timing Chart

Please refer to Timing Chart 5, page 409.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	59.69±0.13	2.35±0.006
С	44.45	1.750
F	8.255	0.325
Н	1.27 (T.P.)	0.050 (T.P.)
ŀ	7.62	0.300
J	2.0	0.079
К	3.18	0.125
L	17.78	0.700
М	25.4	1.000
N	2.45 MAX.	0.097 MAX.
Р	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	0.157+0.005
S	φ1.8	φ0.071
т	1.0±0.1	0.039+0.005
U	3.18 MIN.	0.125 MIN.
٧	0.25 MAX.	0.010 MAX.
w	1.0±0.05	0.039+0.003
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.
		M729-50A4

M72S-50A4



MOS INTEGRATED CIRCUIT MC-42S2000LAB32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S2000LAB32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μ PD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- CAS before RAS self refresh, CAS before RAS refresh, RAS only refresh, Hidden refresh
- · 2,097,152 words by 32 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time		onsumption MAX.)
,	(MAX.)	(MIN.)	Active	Standby
MC-42S2000LAB32S-A60	60 ns	110 ns	1,440 mW	
MC-42S2000LAB32S-A70	70 ns	130 ns	1,296 mW	2.16 mW (CMOS level input)
MC-42S2000LAB32S-A80	80 ns	150 ns	1,152 mW	- (Civios level llipat)

- · 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

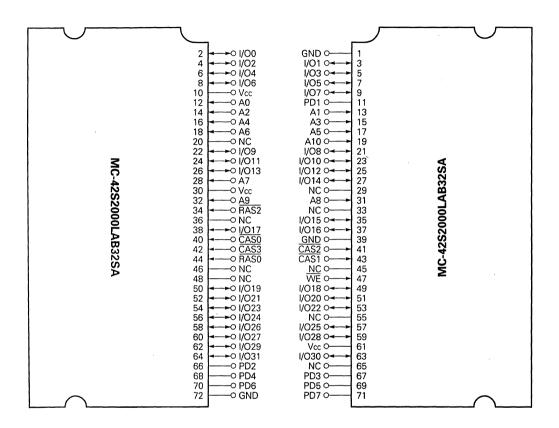
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module	4 pieces of μPD42S17800LG5
MC-42S2000LAB32SA-A70	70 ns	(Socket Type)	(400 mil TSOP (II))
MC-42S2000LAB32SA-A80	80 ns	Edge connector: Gold plating	[Single side]

The information in this document is subject to change without notice.

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plating)



A0 - A10

: Address Inputs

I/O0 - I/O31 RAS0, RAS2 : Data Inputs/Outputs: Row Address Strobe

CASO - CAS3

: Column Address Strobe

WE

: Write Enable

PD1 - PD7

: Presence Detect Pins

Vcc

: Power Supply

GND

: Ground

NC

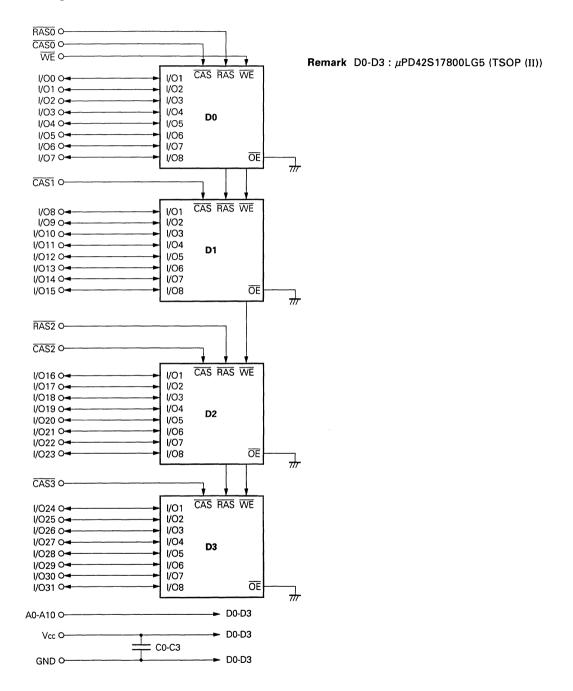
: No connection

The internal connection of PD pins (PD1 to PD7).

Pin	Pin	Access Time					
Name	No.	o. 60 ns 70 ns		80 ns			
PD1	11	GND	GND	GND			
PD2	66	NC	NC	NC			
PD3	67	GND	GND	GND			
PD4	68	NC	NC	NC			
PD5	69	NC	GND	NC			
PD6	70	NC	NC	GND			
PD7	71	GND	GND	GND			



Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vт		-0.5 to +4.6	V
Supply voltage	Vcc		-0.5 to +4.6	. V
Output current	lo		20	mA
Power dissipation	Po		4	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	V
High level input voltage	Vıн		2.0		Vcc + 0.3	٧
Low level input voltage	VIL		-0.3		+0.8	V
Operating ambient temperature	TA		0		70	°C

Capacitance (TA = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A10			35	pF
	Cı2	WE			43	
	Сіз	RASO, RAS2			30	
	C14	CASO - CAS3			17	
Data Input/Output capacitance	Cı/o	I/O0 - I/O31			12	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling	trac = 60 ns		400	mA	3, 4, 7
		trc = trc (MIN.)	trac = 70 ns		360		
		lo = 0 mA	trac = 80 ns		320		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		2.0	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		0.6		
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		400	mA	3, 4, 5, 7
		CAS ≥ Vih (MIN.)	trac = 70 ns		360		
		trc = trc (MIN.) lo = 0 mA	trac = 80 ns		320		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		280	mA	3, 4, 6
(Fast page mode)		tpc = tpc (MIN.)	trac = 70 ns		240		
		lo = 0 mA	trac = 80 ns		200	İ '	
CAS before RAS	Icc5	RAS Cycling	trac = 60 ns		400	mA	3, 4
refresh current		trc = trc (MIN.)	trac = 70 ns		360		
		lo = 0 mA	trac = 80 ns		320		
CAS before RAS long refresh current	Icce		tras ≤ 1 <i>μ</i> s		800	μΑ	3, 4
CAS before RAS self refresh current	Icc7	$\label{eq:rass} \begin{split} \overline{RAS}, \overline{CAS}\colon \\ t_{RASS} &= 5 \text{ ms} \\ \text{Vcc} -0.2 \text{ V} \leq \text{Vih} \leq \text{Vih (MAX.)} \\ 0 \text{ V} \leq \text{Vil} \leq 0.2 \text{ V} \\ \text{Io} &= 0 \text{ mA} \end{split}$			600	μΑ	4
Input leakage current	lı (L)	V _I = 0 to 3.6 V All other pins not under test	= 0 V	-5	+5	μА	
Output leakage current	lo (L)	Vo = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μА	
High level output voltage	Vон	lo = −2.0 mA		2.4		٧	
Low level output voltage	Vol	lo = +2.0 mA			0.4	V	



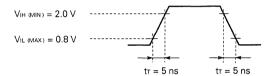
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

	Symbol	trac = 60 ns		trac = 70 ns		trac = 80 ns			
Parameter		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Access Time from RAS	t RAC		60		70		80	ns	10, 11
Access Time from CAS	tcac		15		18		20	ns	10, 11
Access Time Column Address	taa		30		35		40	ns	10, 11
Access Time from CAS Precharge	t ACP		35		40		45	ns	11
RAS to Column Address Delay Time	TRAD	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	tre	40		50		60		ns	
RAS Pulse Width	TRAS	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	TRASP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tяsн	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tcsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tone	5		5		5		ns	13
CAS Precharge Time	torn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	tapc	5		5		5		ns	
RAS Hold Time from CAS Precharge	truce	35		40		45		ns	
Row Address Setup Time	tasa	0		0		0		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twcн	10		10		15		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsr	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
RAS Pulse Width (CAS before RAS Self Refresh)	trass	100		100		100		μs	
RAS Precharge Time (CAS before RAS Self Refresh)	trps	110		130		150		ns	
CAS Hold Time (CAS before RAS Self Refresh)	tchs	-50		-50		-50		ns	
WE Setup Time	twsn	10		10		10	****	ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	TREF		128		128		128	ms	

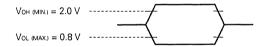


Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4, Icc5 and Icc6 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition
 - (1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (MAX.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

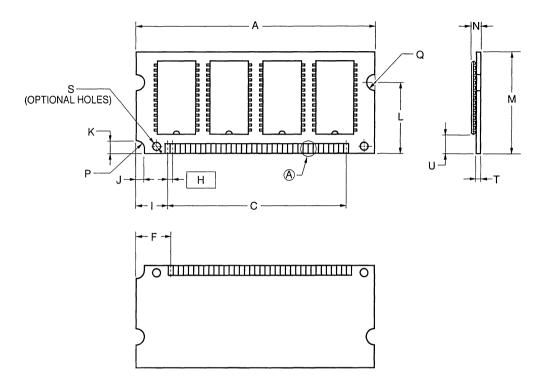
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tds (MIN.) and tdh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

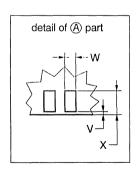
Timing Chart

Please refer to Timing Chart 6, page 419.

Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	59.69±0.13	2.35±0.006
С	44.45	1.750
F	8.255	0.325
Н	1.27 (T.P.)	0.050 (T.P.)
1	7.62	0.300
J	2.03±0.13	$0.080\substack{+0.005 \\ -0.006}$
K	3.175±0.13	0.125±0.006
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	2.463 MAX.	0.097 MAX.
Р	R2.0	R0.079
Q	R2.0	R0.079
S	φ1.8	ϕ 0.071
Т	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A1-2



MOS INTEGRATED CIRCUIT MC-42S2000LAD32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S2000LAD32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μ PD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- CAS before RAS self refresh, CAS before RAS refresh, RAS only refresh, Hidden refresh
- · 2,097,152 words by 32 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time (MIN.)	Power consumption (MAX.)		
·	(MAX.)	(IVIIIV.)	Active	Standby	
MC-42S2000LAD32S-A60	60 ns	110 ns	1,083.6 mW		
MC-42S2000LAD32S-A70	70 ns	130 ns	1,011.6 mW	2.16 mW (CMOS level input)	
MC-42S2000LAD32S-A80	80 ns	150 ns	939.6 mW	Civico level input/	

- · 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

The information in this document is subject to change without notice.



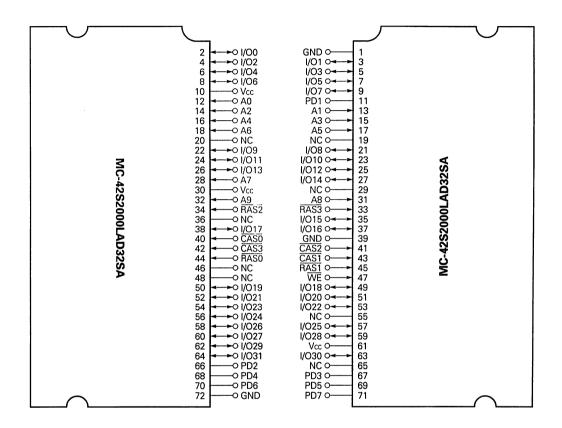
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module	4 pieces of μPD42S18160LG5
MC-42S2000LAD32SA-A70	70 ns	(Socket Type)	(400 mil TSOP (II))
MC-42S2000LAD32SA-A80	80 ns	Edge connector: Gold plating	[Double side]



Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



 A0 - A9
 : Address Inputs

 I/O0 - I/O31
 : Data Inputs/Outputs

 RAS0 - RAS3
 : Row Address Strobe

 CAS0 - CAS3
 : Column Address Strobe

WE : Write Enable

PD1 - PD7 : Presence Detect Pins

: No connection

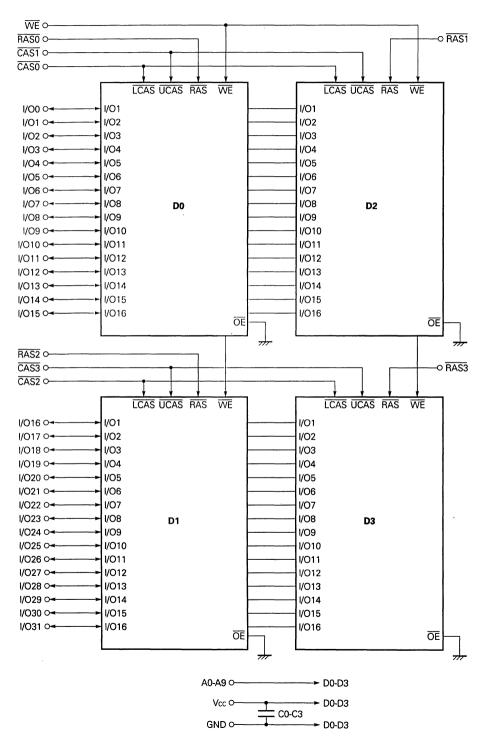
Vcc : Power Supply GND : Ground

NC

The internal connection of PD pins (PD1 - PD7).

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD1	11	NC	NC	NC		
PD2	66	GND	GND	GND		
PD3	67	GND	GND	GND		
PD4	68	GND	GND	GND		
PD5	69	NC	GND	NC		
PD6	70	NC	NC	GND		
PD7	71	GND	GND	GND		

Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-0.5 to +4.6	V
Supply voltage	Vcc		-0.5 to +4.6	V
Output current	lo		20	mA
Power dissipation	Po		8	w
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tatg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	٧
High level input voltage	ViH		2.0		Vcc + 0.3	٧
Low level input voltage	VIL		-0.3		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cn	A0 - A9			35	
	Cı2	WE			43	_
	Сіз	RAS0 - RAS3			23	pF
	Ci4	CASO - CAS3			24	
Data Input/Output capacitance	Cı/o	I/O0 - I/O31			19	рF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling	trac = 60 ns		301		
		trc = trc (MIN.)	trac = 70 ns		281	mA	3, 4, 7
		lo = 0 mA	trac = 80 ns		261		
Standby current	lcc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		2.0	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		0.6		
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		301		
		CAS ≥ Vih (MIN.) trc = trc (MIN.)	trac = 70 ns		281	mA	3, 4, 5, 7
		lo = 0 mA	trac = 80 ns		261		
Operating current	lcc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		181		
(Fast page mode)		tpc = tpc (MIN.)	trac = 70 ns		161	mA	3, 4, 6
		lo = 0 mA	trac = 80 ns		141		
CAS before RAS	lcc5	RAS Cycling	trac = 60 ns		301		
rofresh current		trc = trc (MIN.)	trac = 70 ns		281 mA		3, 4
		lo = 0 mA	trac = 80 ns	261			
CAS before RAS long refresh current	Icce	TAS before RAS refresh: tnc = 125.0 µs RAS, CAS: Vcc -0.2 V ≤ ViH ≤ ViH (MAX.) 0 V ≤ ViL ≤ 0.2 V Standby: RAS, CAS ≥ Vcc -0.2 V Address: ViH or ViL WE: ViH lo = 0 mA	tras ≤ 1 µs		720	μΑ	3, 4
CAS before RAS self refresh current	Icc7	$\label{eq:ranking_ranking} \begin{split} \overline{\text{RAS}}, \overline{\text{CAS}}: \\ \text{trass} &= 5 \text{ ms} \\ \text{Vcc} &-0.2 \text{ V} \leq \text{V}_{\text{IH}} \leq \text{V}_{\text{IH}} \text{ (MAX.)} \\ \text{0 V} &\leq \text{V}_{\text{IL}} \leq 0.2 \text{ V} \\ \text{Io} &= 0 \text{ mA} \end{split}$		600	μΑ	4	
Input leakage current	lı (L)	V _I = 0 to 3.6 V All other pins not under test	-5	+5	μА		
Output leakage current	lo (L)	Vo = 0 to 3.6 V Output is disabled (Hi-Z)	-5	+5	μА		
High level output voltage	Vон	lo = −2.0 mA		2.4		٧	
Low level output voltage	Vol	lo = +2.0 mA			0.4	V	



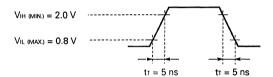
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

	trac = 60 ns		trac = 70 ns		trac = 80 ns				
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Access Time from RAS	TRAC		60		70		80	ns	10, 11
Access Time from CAS	tcac		15		20		20	ns	10, 11
Access Time Column Address	taa		30		35		40	ns	10, 11
Access Time from CAS Precharge	tacp		35		40		45	ns	11
RAS to Column Address Delay Time	TRAD	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcız	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	tт	3	50	3	50	3	50	ns	
RAS Precharge Time	t RP	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	trsh	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	tcsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	5		5		5		ns	
RAS Hold Time from CAS Precharge	TRHCP	35		40		45		ns	
Row Address Setup Time	tasr	0		0		0		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcan	15		15		15		ns	
Column Address Lead Time Referenced to RAS	TRAL	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	tarh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twcн	10		10		15		ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsa	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
RAS Pulse Width (CAS before RAS Self Refresh)	trass	100		100		100		μs	
RAS Precharge Time (CAS before RAS Self Refresh)	trps	110		130		150		ns	
CAS Hold Time (CAS before RAS Self Refresh)	tcнs	-50		-50		-50		ns	
WE Hold Time	twhr	15		15		15		ns	
Refresh Time	tref		128		128		128	ms	

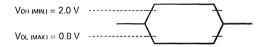


Notes

- 1. All voltages are referenced to GND.
- 3. Icc1, Icc3, Icc4, Icc5 and Icc6 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume tr = 5 ns.
- 9. AC Characteristics test condition
 - (1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and tred ≤ tred (MAX.)	taa (max.)	trad + taa (MAX.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

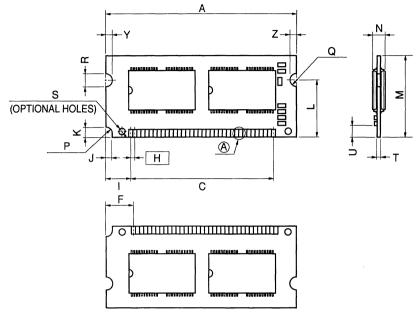
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

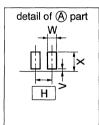
Timing Chart

Please refer to Timing Chart 5, page 409.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	59.69±0.13	2.35±0.006
С	44.45	1.750
F	8.255	0.325
Н	1.27 (T.P.)	0.050 (T.P.)
1	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
М	25.4	1.000
N	3.8 MAX.	0.150 MAX.
Р	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	0.157+0.005
S	φ1.8	ϕ 0.071
Т	1.0±0.1	0.039+0.005
U	3.18 MIN.	0.125 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039+0.003
X	2.54 MIN.	0.100 MIN.
Υ	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.
		M72S-50A3



MOS INTEGRATED CIRCUIT MC-42S4000LAB32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAB32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μ PD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- CAS before RAS self refresh, CAS before RAS refresh, RAS only refresh, Hidden refresh
- · 4,194,304 words by 32 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time (MIN.)	Power consumption (MAX.)		
,	(MAX.)	(WIIN.)	Active	Standby	
MC-42S4000LAB32S-A60	60 ns	110 ns	1,458 mW		
MC-42S4000LAB32S-A70	70 ns	130 ns	1,314 mW	4.32 mW (CMOS level input)	
MC-42S4000LAB32S-A80	80 ns	150 ns	1,170 mW	(Cirios level llipat)	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

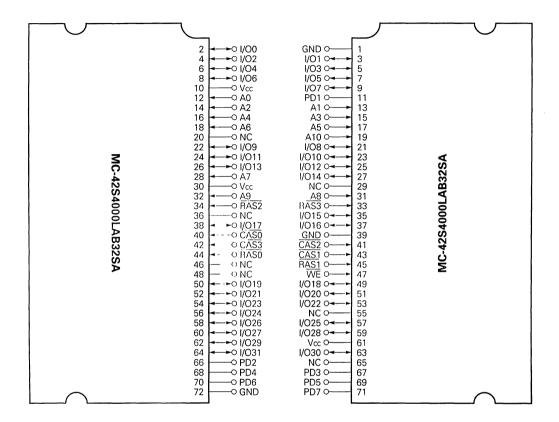
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module	8 pieces of μPD42S17800LG5
MC-42S4000LAB32SA-A70	70 ns	(Socket Type)	(400 mil TSOP (II))
MC-42S4000LAB32SA-A80	80 ns	Edge connector: Gold plating	[Double side]

The information in this document is subject to change without notice.

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



A0 - A10

: Address Inputs

I/O0 - I/O31

: Data Inputs/Outputs

RAS0 - RAS3

: Row Address Strobe

CASO - CASS

now Address Strobe

WE

: Column Address Strobe

WE

: Write Enable

PD1 - PD7

: Presence Detect Pins

Vcc

: Power Supply

GND

: Ground

NC

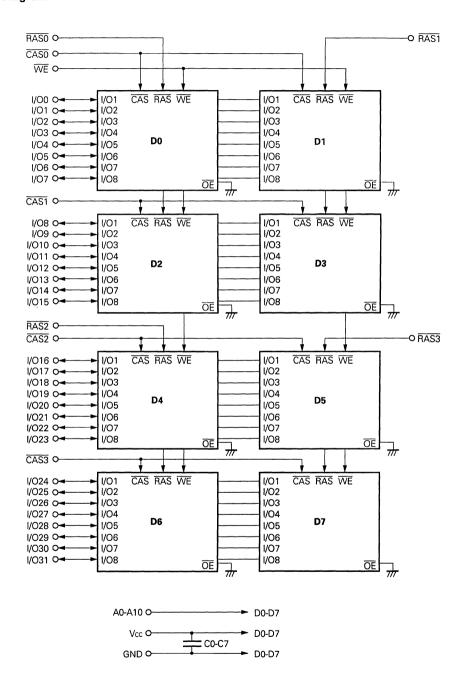
: No connection

The internal connection of PD pins (PD1 to PD7).

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD1	11	GND	GND	GND		
PD2	66	NC	NC	NC		
PD3	67	GND	GND	GND		
PD4	68	GND	GND	GND		
PD5	69	NC	GND	NC		
PD6	70	NC	NC	GND		
PD7	71	GND	GND	GND		



Block Diagram



Remark D0-D7: μPD42S17800LG5 (TSOP (II))



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-0.5 to +4.6	· V
Supply voltage	Vcc		-0.5 to +4.6	V
Output current	lo		. 20	mA
Power dissipation	Po		8	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	٧
High level input voltage	Vін		2.0		Vcc + 0.3	٧
Low level input voltage	VIL		-0.3		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance ($T_A = 25$ °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cn	A0 - A10			55	pF
	Cı2	WE			71	
	Сіз	RASO - RAS3			30	
	C14	CASO - CAS3			24	
Data Input/Output capacitance	Cı/o	I/O0 - I/ O31			19	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling trac = 60 ns			405	mA	3, 4, 7
		trc = trc (MIN.)	trac = 70 ns		365		
		lo = 0 mA	trac = 80 ns		325		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo = 0 mA		4.0	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		1.2		
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		405	mA	3, 4, 5, 7
		CAS ≥ Vih (MIN.)	trac = 70 ns		365		
		trc = trc (MIN.) lo = 0 mA	trac = 80 ns		325		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac :: 60 ns		285	mA	3, 4, 6
(Fast page mode)		tpc = tpc (MIN.)	teac :: 70 ns		245		
		lo = 0 mA	teac = 80 ns		205		
CAS before RAS	lcc5	RAS Cycling	trac = 60 ns		405	mA	3, 4
refresh current		trc = trc (MIN.)	trac - 70 ns		365		
		lo = 0 mA	trac - 80 ns		325		
CAS before RAS long refresh current	Icce		tras ≤ 1 µs		1.6	mA	3, 4
CAS before RAS self refresh current	Icc7	$\label{eq:rass} \begin{array}{l} \overline{RAS}, \overline{CAS}\colon \\ \text{trass} = 5 \text{ms} \\ \text{Vcc} -0.2 \text{V} \leq \text{Vih} \leq \text{Vih} (\text{MAX.}) \\ 0 \text{V} \leq \text{Vil.} \leq 0.2 \text{V} \\ \text{lo} = 0 \text{mA} \end{array}$			1.2	mA	4
Input leakage current	lı (L)	V _I = 0 to 3.6 V All other pins not under test	= 0 V	- 5	+5	μΑ	
Output leakage current	lo (L)	Vo = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μА	
High level output voltage	Vон	lo = -2.0 mA		2.4		V	
Low level output voltage	Vol	lo = +2.0 mA			0.4	V	-



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

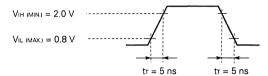
		TRAC	= 60 ns	trac = 70 ns		60 ns trac = 70 r		= 70 ns trac = 80 ns]	
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes		
Read/Write Cycle Time	trc	110		130		150		ns	 		
Fast Page Mode Cycle Time	tpc	40		45		50		ns			
Access Time from RAS	trac		60		70		80	ns	10, 11		
Access Time from CAS	tcac		15		18		20	ns	10, 11		
Access Time Column Address	. taa		30		35		40	ns	10, 11		
Access Time from CAS Precharge	tacp		35		40		45	ns	11		
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10		
CAS to Data Setup Time	tcLz	0		0		0		ns	11		
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12		
Transition Time (Rise and Fall)	t⊤	3	50	3	50	3	50	ns			
RAS Precharge Time	trp	40		50		60		ns			
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns			
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns			
RAS Hold Time	i rsh	15		18		20		ns			
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns			
CAS Hold Time	tcsн	60		70		80		ns			
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10		
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13		
CAS Precharge Time	tcpn	10		10		10		ns			
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns			
RAS Precharge CAS Hold Time	trpc	5		5		5		ns			
RAS Hold Time from CAS Precharge	trhcp	35		40		45		ns			
Row Address Setup Time	tasa	0		0		0		ns			
Row Address Hold Time	trah	10		10		12		ns	l .		
Column Address Setup Time	tasc	0		0		0		ns			
Column Address Hold Time	tcah	15		15		15		ns			
Column Address Lead Time Referenced to RAS	TRAL	30		35		40		ns			
Read Command Setup Time	trcs	0		0		0		ns			
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14		
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14		
WE Hold Time Referenced to CAS	twcн	10		10		15		ns	15		
Data-in Setup Time	tos	0		0		0		ns	16		
Data-in Hold Time	tон	10		15		15		ns	16		
Write Command Setup Time	twcs	0		0		Ó		ns	17		
CAS Setup Time (CAS before RAS Refresh)	tcsr	5		5		5		ns			
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns			
RAS Pulse Width (CAS before RAS Self Refresh)	trass	100		100		100		μs			
RAS Precharge Time (CAS before RAS Self Refresh)	trps	110		130		150		ns			
CAS Hold Time (CAS before RAS Self Refresh)	tcнs	-50		-50		-50		ns			
WE Setup Time	twsn	10		10		10		ns			
WE Hold Time	twnr	15		15		15		ns			
Refresh Time	TREF		128		128		128	ms			



Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4, Icc5 and Icc6 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification

10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	trac (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (MAX.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions $trad \ge trad (MAX.)$ and $trad \ge trad (MAX.)$ will not cause any operation problems.

- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

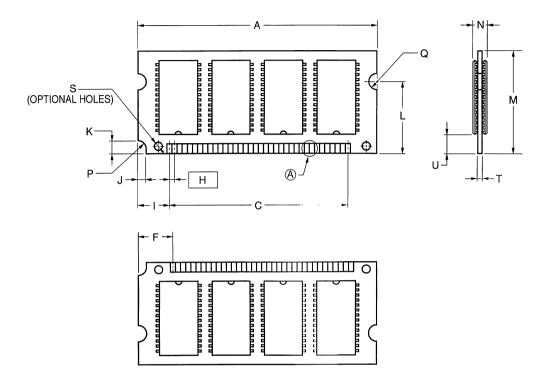
Timing Chart

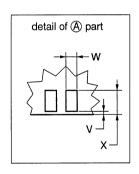
Please refer to Timing Chart 6, page 419.



Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	59.69±0.13	2.35±0.006
С	44.45	1.750
F	8.255	0.325
Н	1.27 (T.P.)	0.050 (T.P.)
- 1	7.62	0.300
J	2.03±0.13	$0.080\substack{+0.005 \\ -0.006}$
K	3.175±0.13	0.125±0.006
L	17.78	0.700
М	25.4±0.13	1.000±0.006
N	3.81 MAX.	0.150 MAX.
Р	R2.0	R0.079
Q	R2.0	R0.079
S	φ1.8	φ0.071
Т	1.0±0.1	0.039+0.005
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
Х	2.54 MIN.	0.100 MIN.
		MAZOC EDAD O

M72S-50A2-2





MOS INTEGRATED CIRCUIT MC-42S4000LAC32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAC32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μ PD42S17400LG3 (TSOP (II)) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- CAS before RAS self refresh, CAS before RAS refresh, RAS only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- · Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	1	onsumption //AX.)
,	(IVIAA.)	(IVIIIV.)	Active	Standby
MC-42S4000LAC32S-A60	60 ns	110 ns	2,880 mW	
MC-42S4000LAC32S-A70	70 ns	130 ns	2,592 mW	4.32 mW (CMOS level input)
MC-42S4000LAC32S-A80	80 ns	150 ns	2,304 mW	Comou lever input,

- · 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply



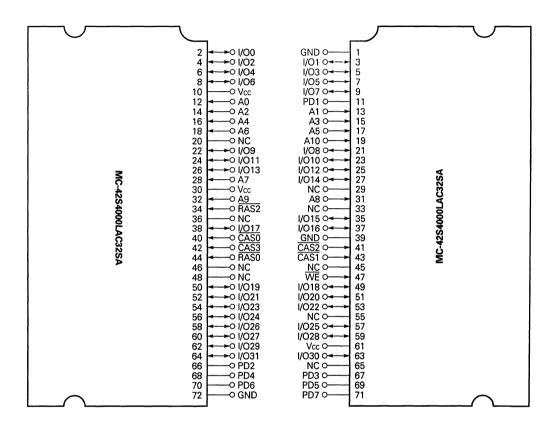
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAC32SA-A60	60 ns	72-pin Dual In-line Memory Module	8 pieces of μPD42S17400LG3
MC-42S4000LAC32SA-A70	70 ns	(Socket Type)	(300 mil TSOP (II))
MC-42S4000LAC32SA-A80	80 ns	Edge connector: Gold plating	[Double side]



Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



A0 - A10 : Address Inputs

I/O0 - I/O31 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

CAS0 - CAS3 : Column Address Strobe

WE : Write Enable

PD1 - PD7 : Presence Detect Pins

Vcc : Power Supply GND : Ground

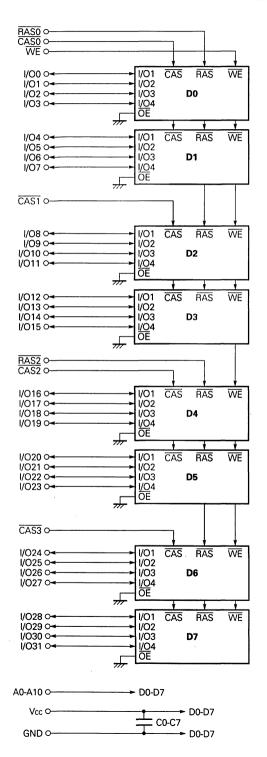
NC: No connection

The internal connection of PD pins (PD1 to PD7).

Pin	Pin	Access Time			
Name	No.	60 ns	70 ns	80 ns	
PD1	11	NC	NC	NC	
PD2	66	NC	NC	NC	
PD3	67	GND	GND	GND	
PD4	68	NC	NC	NC	
PD5	69	NC	GND	NC	
PD6	70	NC	NC	GND	
PD7	71	GND	GND	GND	

Block Diagram

Remark D0-07: μ PD42S17400LG3 (TSOP (II))





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vt		-0.5 to +4.6	٧
Supply voltage	Vcc		-0.5 to +4.6	٧
Output current	lo		20	mA
Power dissipation	Рь		8	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	٧
High level input voltage	ViH		2.0		Vcc + 0.3	٧
Low level input voltage	VIL		-0.3		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A10			55	
	Cı2	WE			71	
	Сіз	RASO, RAS2			36	pF
	C ₁₄	CASO - CAS3			19	
Data Input/Output capacitance	Ci/o	I/O0 - I/O31			10	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling	trac = 60 ns		800		
!		trc = trc (MIN.)	trac = 70 ns		720	mA	3, 4, 7
,		lo = 0 mA	trac = 80 ns		640		
Standby current	lcc2	RAS, CAS ≥ V _{IH} (MIN.) Io = 0 r			4	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo = 0 mA		1.2	'''	
RAS only refresh current	Іссз	RAS Cycling	trac = 60 ns		800		
		CAS ≥ VIH (MIN.)	trac = 70 ns		720	mA	3, 4, 5, 7
		trc = trc (MIN.) lo = 0 mA	trac = 80 ns		640		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling	trac = 60 ns		560		
(Fast page mode)		tpc = tpc (MIN.)	trac = 70 ns		480	mA	3, 4, 6
		lo = 0 mA	trac = 80 ns		400		
CAS before RAS	Icc5	RAS Cycling	trac = 60 ns		800		
refresh current		trc = trc (MIN.)	trac = 70 ns		720	mA	3, 4
		lo = 0 mA	trac = 80 ns		640		
CAS before RAS long refresh current	Iccs	$\overline{\text{CAS}} \text{ before } \overline{\text{RAS}} \text{ refresh:}$ $\frac{\text{trc} = 62.5 \ \mu\text{s}}{\text{RAS, CAS}:}$ $\text{Vcc} -0.2 \ \text{V} \le \text{ViH} \le \text{ViH} \ \text{(MAX.)}$ $0 \ \text{V} \le \text{ViL} \le 0.2 \ \text{V}$ Standby: $\overline{\text{RAS}} \ge \text{Vcc} -0.2 \ \text{V}$ $\text{Address: ViH or ViL}$ $\overline{\text{WE}: \text{ViH}}$ $\text{Io} = 0 \ \text{mA}$	tras ≤ 1 μs		1.6	mA	3, 4
CAS before RAS self refresh current	Icc7	RAS, CAS: trass = 5 ms $Vcc -0.2 \text{ V} \leq \text{Vih} \leq \text{Vih (MAX.)}$ $0 \text{ V} \leq \text{Vil} \leq 0.2 \text{ V}$ $lo = 0 \text{ mA}$			1.2	mA	4
Input leakage current	lı (L)	V _I = 0 to 3.6 V All other pins not under test = 0 V		-5	+5	μА	
Output leakage current	lo (L)	Vo = 0 to 3.6 V Output is disabled (Hi-Z)		-5	+5	μА	
High level output voltage	Vон	lo = -2.0 mA		2.4		٧	
Low level output voltage	Vol	lo = +2.0 mA			0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

		trac	= 60 ns	TRAC	= 70 ns	TRAC	= 80 ns	·	T.,
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		15		18		20	ns	10, 11
Access Time Column Address	taa		30		35		40	ns	10, 11
Access Time from CAS Precharge	tace		35		40		45	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	trp	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tяsн	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tcsн	60		70		80		ns	
RAS to CAS Delay Time	trico	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	terp	5		5		5		ns	13
CAS Precharge Time	topn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tor	10		10		10		ns	
RAS Precharge CAS Hold Time	tarc	5		5		5		ns	
RAS Hold Time from CAS Precharge	tunce	35		40		45		ns	
Row Address Setup Time	tasa	0		0		0		ns	
Row Address Hold Time	t rah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	t CAH	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15	-,,	ns	15
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0	,	0		ns	17
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
WE Setup Time	twsn	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
RAS Pulse Width (CAS before RAS Self Refresh)	trass	100		100		100		μs	
RAS Precharge Time (CAS before RAS Self Refresh)	trps	110		130		150		ns	
CAS Hold Time (CAS before RAS Self Refresh)	tcнs	-50		-50		-50		ns	
Refresh Time	TREF		128		128		128	ms	

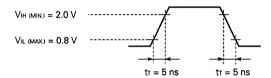
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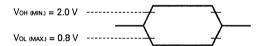
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4, Icc5 and Icc6 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5 \text{ ns}$.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS	
trad ≤ trad (MAX.) and tred ≤ tred (MAX.)	TRAC (MAX.)	TRAC (MAX.)	
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (MAX.)	
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)	

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad (MAX.) and trad ≥ trad (MAX.) will not cause any operation problems.

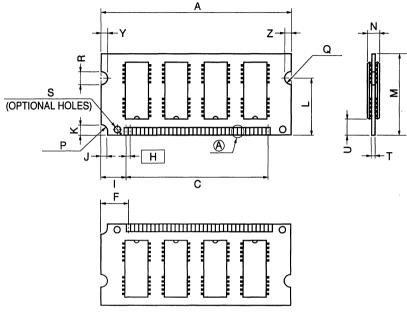
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (мах.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to Voн or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

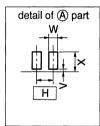
Timing Chart

Please refer to Timing Chart 6, page 419.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
Α	59.69±0.13	2.35±0.006
С	44.45	1.750
F	8.255	0.325
Н	1.27 (T.P.)	0.050 (T.P.)
1	7.62	0.300
J	2.0	0.079
К	3.18	0.125
L	17.78	0.700
М	25.4	1.000
N	3.8 MAX.	0.150 MAX.
Р	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	0.157+0.005
S	φ1.8	φ0.071
Т	1.0±0.1	0.039+0.005
U	3.18 MIN.	0.125 MIN.
٧	0.25 MAX.	0.010 MAX.
w	1.0±0.05	0.039+0.003
Х	2.54 MIN.	0.100 MIN.
Υ	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.
		M72S-50A5

8 Byte DIMM [Fast Page]





MC-421000AA64FA

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA64FA is a 1,048,576 words by 64 bits dynamic RAM module on which 16 pieces of 4 M DRAM: μ PD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time	1	consumption MAX.)
·	(MAX.)	(MIN.)	Active	Standby
MC-421000AA64-60	60 ns	110 ns	10.42 W	
MC-421000AA64-70	70 ns	130 ns	8.74 W	420 mW (CMOS level input)
MC-421000AA64-80	80 ns	150 ns	7.90 W	COMOS level iliput)

- · 1,024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

The information in this document is subject to change without notice.



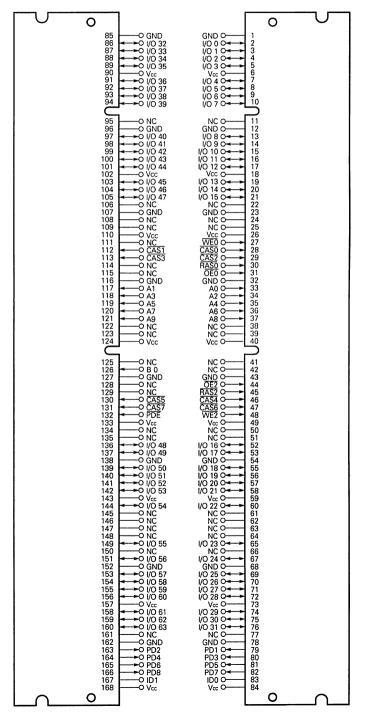
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FA-60	60 ns	168-pin Dual In-line Memory Module	16 pieces of μPD424400LA
MC-421000AA64FA-70	70 ns	(Socket Type)	(300 mil SOJ)
MC-421000AA64FA-80	80 ns	Edge connector: Gold plating	[Double side]



Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD1	79	L	L	L		
PD2	163	L	L	L		
PD3	80	Н	Н	Н		
PD4	164	L	L	L		
PD5	81	L	L	L		
PD6	165	Н	L	Н		
PD7	82	Н	H	L		
PD8	166	Н	Н	Н		
ID0	83	GND	GND	GND		
ID1	167	GND	GND	GND		

Remark H: Voh, L: Vol

A0 - A9, B0 : Address Inputs

1/O 0 - 1/O 63 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

CAS0 - CAS7 : Column Address Strobe

WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

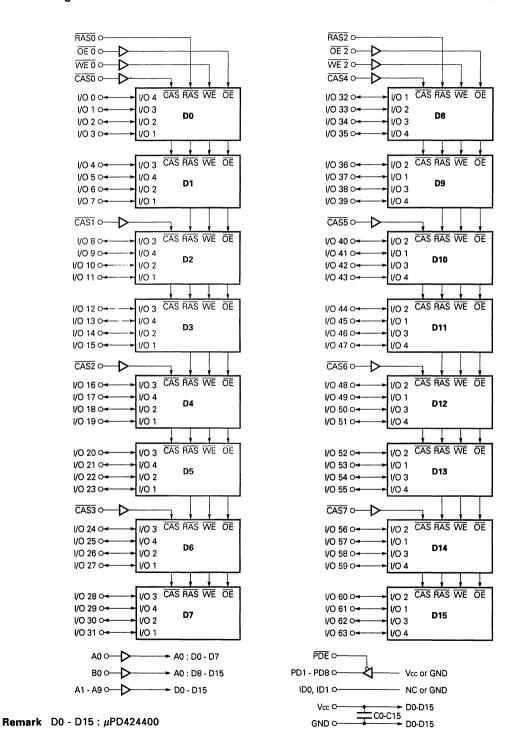
PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

: No connection

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground

NC

Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vt		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Po		18	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cn	A0 - A9, B0			20	
	Cı2	WEO, WE2			20	
	Сіз	RASO, RAS2			78	pF
	C14	CASO - CAS7			20	
	Сіб	OE0, OE2		,	20	
Data Input/Output capacitance	C _{I/O}	I/O0 - I/O63			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling		= 60 ns		1,984		
		trc = trc (MIN.)	TRAC	= 70 ns		1,664	mA	3, 4, 7
		10 = 0 MA	trac	= 80 ns		1,504		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)		0 mA		96	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo =	lo = 0 mA		80	""	
RAS only refresh current	Іссз	RAS Cycling	trac	= 60 ns		1,984		
		trc = trc (MIN.)		trac = 70 ns		1,664	mA	3, 4, 5, 7
				trac = 80 ns		1,504		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling tr		= 60 ns		1,504		
(Fast page mode)			trac = 70 ns			1,344	mA	3, 4, 6
		lo = 0 mA	trac	= 80 ns		1,184		
CAS before RAS	lccs	RAS Cycling	trac	= 60 ns		1,984		
refresh current		tnc = tnc (MIN.)	trac	trac = 70 ns		1,664	mA	3, 4
		lo = 0 mA	trac	trac = 80 ns		1,504		
Input leakage current	lı (L)	V _I = 0 to 5.5 V		RAS	-10	+10		
		All other pins not under test	= 0 V	Othors	-5	+1	μА	÷
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μА		
High level output voltage	Vон	lo = -5.0 mA		2.4		٧		
Low level output voltage	Vol	lo = +4.2 mA				0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

_		trac	= 60 ns	trac	= 70 ns	trac	= 80 ns		Notes
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	
Read/Write Cycle Time	trc	110		130		160		ns	
Read Modify Write Cycle Time	trwc	165		190		225		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	tprwc	80		90		100		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		20		25		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	TACP		40		45		50	ns	11
Access Time from OE	toea		20		25		25	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLz	0		0		0		ns	11
OE to Data Setup Time	touz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
OE to Data Delay Time	toed	15		15		20		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	15	0	15	0	20	ns	12
OE Hold Time	tоен	0		0		0		ns	
OE Lead Time Referenced to RAS	toes	0		0		0		ns	
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	tre	40		50		70		ns	
RAS Pulse Width	TRAS	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tяsн	15		20		20		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	tcsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	10		10		10		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	10		10		10		ns	
RAS Hold Time from CAS Precharge	trhcp	40		45		50		ns	
Row Address Setup Time	tasr	5		5		5		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	t CAH	15		15		15		ns	
Column Address Lead Time Referenced to RAS	TRAL	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrH	0		0		10		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	15		15		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

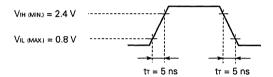


Parameter	Sumbal	trac =	= 60 ns	trac = 70 ns		trac = 80 ns		Unit	Notes
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	ivotes
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	15		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	35		40		45		ns	17
RAS to WE Delay Time	trwo	90		100		115		ns	17
CAS Precharge to WE Delay Time	tcpwd	55		60		70		ns	17
Column Address to WE Delay Time	tawo	55		60		70		ns	17
WE Lead Time Referenced to RAS	trwL	20		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsr	10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		15		ns	
WE Setup Time	twsn	0		0		10		ns	
WE Hold Time	twnr	10		10		15		ns	
Refresh Time	TREF		16		16		16	ms	

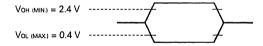


Notes

- 1. All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (trc and trc).
- 4. Specified values are obtained with outputs unloaded.
- 5. lcc3 is measured assuming that all column address inputs are held at either high or low.
- lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition
 - (1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and tred ≤ tred (MAX.)	TAA (MAX.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trod + toac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch (MIN.) should be met.

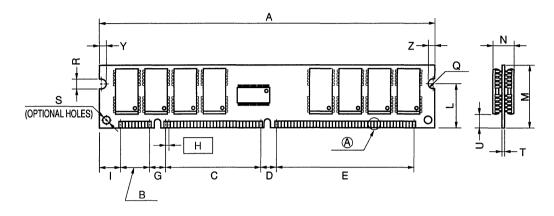
- 16. tos (MIN.) and toh (MIN.) are referenced to the \overline{CAS} falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the \overline{WE} falling edge.
- 17. If twos ≥ twos (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If tRWD ≥ tRWD (MIN.), tcWD ≥ tcWD (MIN.), tAWD ≥ tAWD (MIN.) and tcPWD ≥ tcPWD (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

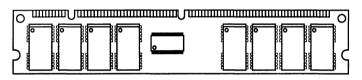
Timing Chart

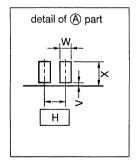
Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
Е	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
ı	8.89	0.350
L	17.78	0.700
М	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157_{-0.004}^{+0.005}$
S	φ3.0	ϕ 0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
w	1.0±0.05	$0.039_{-0.002}^{+0.003}$
X	2.54 MIN.	0.100 MIN.
Υ	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A1

M168S-50A1



MC-421000AA64FB

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μ PD4218160 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time	I	consumption (MAX.)
,	(MAX.)	(MIN.)	Active	Standby
MC-421000AA64-60	60 ns	110 ns	3.68 W	
MC-421000AA64-70	70 ns	130 ns	3.47 W	336 mW (CMOS level input)
MC-421000AA64-80	80 ns	150 ns	3.26 W	(Givies level impat)

- · 1,024 refresh cycles/16 ms
- · CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

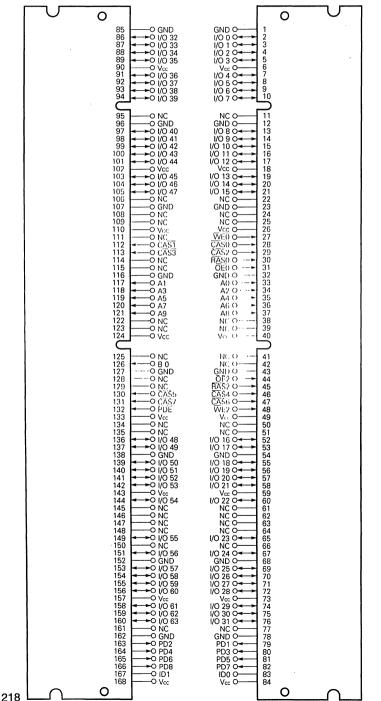
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FB-60	60 ns	168-pin Dual In-line Memory Module	4 pieces of μPD4218160LE
MC-421000AA64FB-70	70 ns	(Socket Type)	(400 mil SOJ)
MC-421000AA64FB-80	80 ns	Edge connector: Gold plating	[Single side]

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	A	cess Tin	ne						
Name	No.	60 ns	70 ns	80 ns						
PD1	79	L	L	L						
PD2	163	L	L	L						
PD3	80	Н	Н	Н						
PD4	164	L	L	L						
PD5	81	L	L	L						
PD6	165	Н	L	Н						
PD7	82	Н	Н	L						
PD8	166	Н	Н	Н						
ID0	83	GND	GND	GND						
ID1	167	GND	GND	GND						

Remark H: Voh, L: Vol

A0 - A9, B0 : Address Inputs

I/O 0 - I/O 63 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

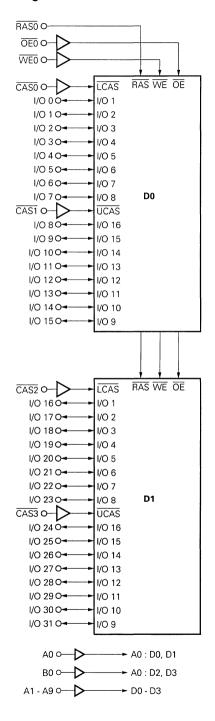
CAS0 - CAS7 : Column Address Strobe

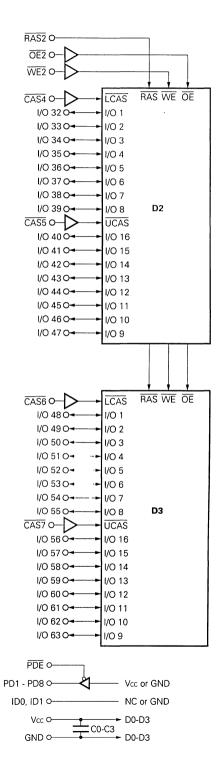
WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram







Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Po		6	w
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A9, B0			20	pF
	Cı2	WEO, WE2			20	
	Сіз	RASO, RAS2			45	
	C14	CASO - CAS7			20	
	Cıs	OE0, OE2			20	
Data Input/Output capacitance	C1/0	I/O0 - I/O63			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc (MIN.) lo = 0 mA	TRAC	= 60 ns = 70 ns = 80 ns		700 660 620	mA	3, 4, 7
Standby current	Icc2	\overline{RAS} , $\overline{CAS} \ge V_{IH (MIN.)}$ \overline{RAS} , $\overline{CAS} \ge V_{CC} - 0.2 \text{ V}$		0 mA		68 64	mA	
RAS only refresh current	Icc3	RAS Cycling CAS ≥ ViH (MIN.) trc = trc (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns		700 660 620	mA	3, 4, 5, 7
Operating current (Fast page mode)	Icc4	RAS VIL (MAX.), CAS Cycling tpc = tpc (MIN.) lo = 0 mA	TRAC	= 60 ns = 70 ns = 80 ns		420 380 340	mA	3, 4, 6
CAS before RAS refresh current	lcc5	RAS Cycling tac = tac (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns		700 660 620	mA	3, 4
Input leakage current	lı (L)	Vi = 0 to 5.5 V All other pins not under test	= 0 V	RAS Others	-10 -5	+10	μА	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)			-10	+10	μА	
High level output voltage	Vон	Io = −2.5 mA		2.4		٧		
Low level output voltage	Vol	lo = +2.1 mA				0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

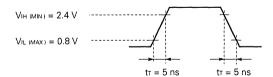
		TRAC	= 60 ns	TRAC	= 70 ns	TRAC	= 80 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Read Modify Write Cycle Time	trwc	173		195		215		ns	
Fast Page Mode Cycle Time	tec	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	terwo	85		90		105		ns	
Access Time from RAS	TRAC		60		70		80	ns	10, 11
Access Time from CAS	tcac		20	1	25		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	TACP		40		45		50	ns	11
Access Time from OE	toea		20		25		25	ns	11
RAS to Column Address Delay Time	TRAD	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tclz	0		0		0		ns	11
OE to Data Setup Time	tolz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
OE to Data Delay Time	toed	13		15		15		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	13	0	15	0	15	ns	12
OE Hold Time	toen	0		0		0		ns	
OE Lead Time Referenced to RAS	toes	0		0		0		ns	
Transition Time (Rise and Fall)	tт	3	50	3	50	3	50	ns	
RAS Precharge Time	tap	40		50		60		ns	
RAS Pulse Width	TRAS	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	TRASP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tasa	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	TRCD	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	TRPC	5		5		5		ns	
RAS Hold Time from CAS Precharge	trhcp	40		45		50		ns	
Row Address Setup Time	tasa	5		5		5		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

8	C	trac :	= 60 ns	trac =	= 70 ns	trac :	= 80 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Data-in Setup Time	tos	0		0	,	0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	38		40		45		ns	17
RAS to WE Delay Time	trwd	93		105		115		ns	17
CAS Precharge to WE Delay Time	tcpwb	60		65		70		ns	17
Column Address to WE Delay Time	tawd	58		65		70		ns	17
WE Lead Time Referenced to RAS	trwL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		15		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	TREF		16		16		16	ms	

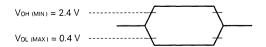
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- 7. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{RAS} \le V_{IL}$ (MAX.) and $\overline{CAS} \ge V_{IH}$ (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification





10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	TRAD + TAA (MAX.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

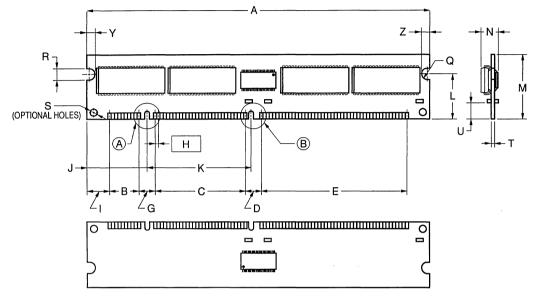
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the \overline{CAS} falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the \overline{WE} falling edge.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If tRWD ≥ tRWD (MIN.), tcWD ≥ tcWD (MIN.), tAWD ≥ tAWD (MIN.) and tcPWD ≥ tcPWD (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

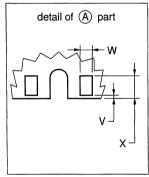
Timing Chart

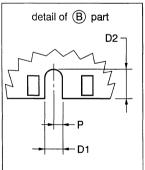
Please refer to Timing Chart 8, page 443.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.05 (T.P.)
1	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
М	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	φ3.0	φ0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039+0.003
Х	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A5



MC-421000AD72F

1 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-421000AD72F is a 1,048,576 words by 72 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μ PD4218160 and 2 pieces of 4 M DRAM: μ PD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 72 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time (MIN.)	1	onsumption MAX.)
·	(MAX.)		Active	Standby
MC-421000AD72-60	60 ns	110 ns	4.94 W	
MC-421000AD72-70	70 ns	130 ns	4.52 W	347 mW (CMOS level input)
MC-421000AD72-80	80 ns	150 ns	4.20 W	

- · 1,024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Moun	nted devices
MC-421000AD72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type)	4 pieces of	μPD4218160G5 (400 mil TSOP(II))
MC-421000AD72F-70	70 ns	Edge connector: Gold plating		and μPD424400G3
MC-421000AD72F-80	80 ns		[Double side	(300 mil TSOP(II))

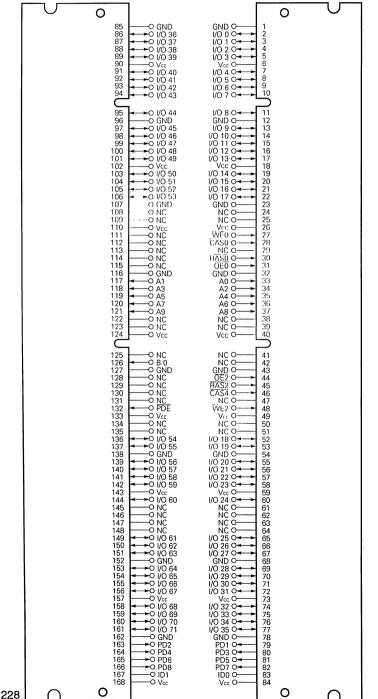
The information in this document is subject to change without notice.

D-3602 (Japan)



Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Ad	cess Tin	ne
Name	No.	60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	Н	Н	Н
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	Н	L	Н
PD7	82	Н	Н	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H: Voh, L: Vol

A0 - A9, B0 : Address Inputs

I/O 0 - I/O 71 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

CAS0, CAS4 : Column Address Strobe

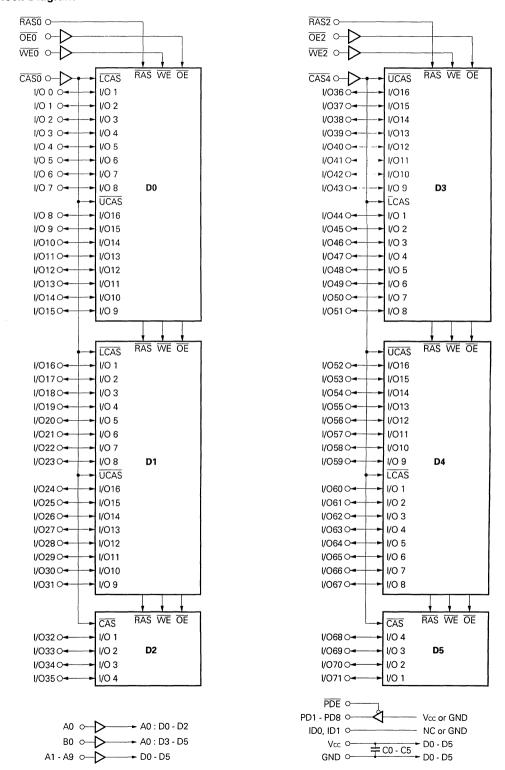
WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection



Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Po		8	w
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	:c

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	Vih		2.4		Vcc + 1.0	٧
Low level input voltage	Vil		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (TA = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cn	A0 - A9, B0			20	pF
	C12	WE0, WE2			20	
	Сіз	RASO, RAS2			36	
	C14	CASO, CAS4			20	
	C ₁₅	OE0, OE2			20	
Data Input/Output capacitance	Ci/o	1/00 - 1/071			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling trc = trc (MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns		940 860 800	mA	3, 4, 7
Standby current	Icc2	\overline{RAS} , $\overline{CAS} \ge V_{IH (MIN.)}$ \overline{RAS} , $\overline{CAS} \ge V_{CC} - 0.2 V$	lo = 0 mA		72 66	mA	
RAS only refresh current	Icc3	RAS Cycling CAS ≥ Viн (MIN.) tnc = tnc (MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac = 80 ns		940 860 800	mA	3, 4, 5, 7
Operating current (Fast page mode)	Icc4	RAS VIL (MAX.), CAS Cycling tpc = tpc (MIN.) lo = 0 mA	trac = 60 ns trac = 70 ns trac - 80 ns		600 540 480	mA	3, 4, 6
CAS before RAS refresh current	Icc5	RAS Cycling trc = trc (MIN.) lo = 0 mA	tвас 60 ns tвас 70 ns tвас 80 ns		940 860 800	mA	3, 4
Input leakage current	lı (L)	V _I = 0 to 5.5 V All other pins not under test	RAS Others	10 5	+10	μА	No. 1
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)	•	10	+10	μΑ	
High level output voltage	Vон	lo = −2.5 mA		2.4		٧	
Low level output voltage	Vol	lo = +2.1 mA			0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

_		t RAC	= 60 ns	trac	= 70 ns	trac = 80 ns			Natar
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		160		ns	
Read Modify Write Cycle Time	trwc	173		195		225		ns	
Fast Page Mode Cycle Time	tpc	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	tprwc	85		90		105		ns	
Access Time from RAS	TRAC		60		70		80	ns	10, 11
Access Time from CAS	tcac		20		25		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	tace		40		45		50	ns	11
Access Time from OE	toea		20		25		25	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLZ	0		0		0		ns	11
OE to Data Setup Time	torz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
OE to Data Delay Time	toed	15		15		20		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	15	0	15	0	20	ns	12
OE Hold Time	tоен	0		0		0		ns	
OE Lead Time Referenced to RAS	toes	0		0		0		ns	
Transition Time (Rise and Fall)	tт	3	50	3	50	3	·50	ns	
RAS Precharge Time	trp	40		50		70		ns	
RAS Pulse Width	tras	60	10,000	. 70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tяsн	15		20		20		ns	
CAS Pulse Width	tcas	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcap	10		10		10		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	10		10		10		ns	
RAS Hold Time from CAS Precharge	trhcp	40		45		50		ns	
Row Address Setup Time	tasa	5		5		5		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		10		ns	14
Read Command Hold Time Referenced to CAS	tясн	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	15		15		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

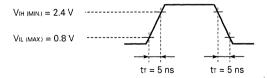


Parameter	Symbol	trac =	= 60 ns	trac =	= 70 ns	trac =	= 80 ns	Unit	Notes
rarameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Onit	notes
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	38		40		45		ns	17
RAS to WE Delay Time	trwo	93		105		115		ns	17
CAS Precharge to WE Delay Time	tcpwb	60		65		70		ns	17
Column Address to WE Delay Time	tawd	58		65		70		ns	17
WE Lead Time Referenced to RAS	trwL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsn	10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
WE Setup Time	twsn	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	TREF		16		16		16	ms	

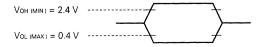
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. lcc1, lcc3, lcc4 and lcc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. lcc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- lcc1 and lcc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification





10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	trac (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trod + toac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

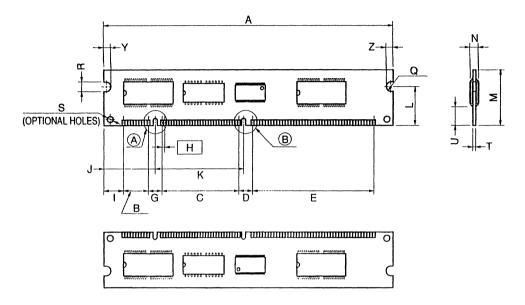
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
- 17. If twos ≥ twos (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If tRWD ≥ tRWD (MIN.), tCWD ≥ tCWD (MIN.), tAWD ≥ tAWD (MIN.) and tCPWD ≥ tCPWD (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

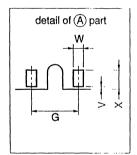
Timing Chart

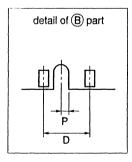
Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
1	8.89	0.350
J	23.495	0.925
К	42.18	1.661
L	17.78	0.700
М	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	0.157+0.005
S	ø3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A4

M168S-50A



MC-422000AA64FB

2M -WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000AA64FB is a 2 097 152 words by 64 bits dynamic RAM module on which 8 pieces of 16M DRAM (μ PD 4218160) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2 097 152 words by 64 bits organization
- Fast access and cycle time

Family	Access time	R/W cycle time	Power cor (MA)	nsumption K.)
	(MAX.)	(MIN.)	Active	Standby
MC- 422000AA64-60	60ns	110ns	3.74 w	
MC- 422000AA64-70	70ns	130ns	3.53 w	378 mW
MC- 422000AA64-80	80ns	150ns	3.32 w	(CMOS level)

- 1 024 refresh cycles/16 ms
- CAS before RAS refresh , RAS only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single $+5.0V \pm 0.25V$ power supply

The information in this document is subject to change without notice.

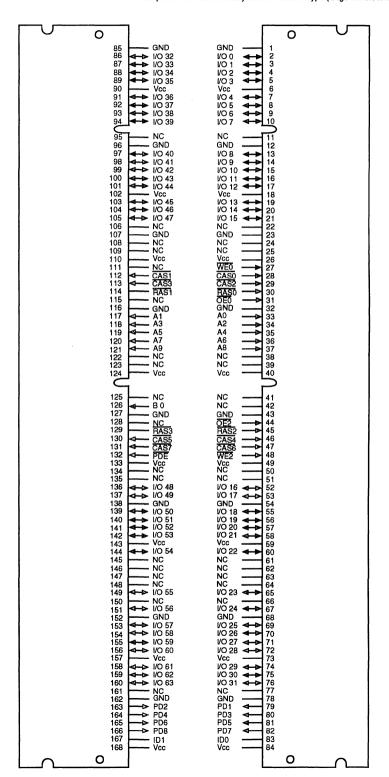
D-3612A (Japan) 237

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 422000AA64FB-60	60ns	168-pin Dual In-line	8 pieces of
MC- 422000AA64FB-70	70ns	Memory Module (Socket Type)	uPD 4218160LE
MC- 422000AA64FB-80	80ns	Edge connector: Gold plating	(400mil SOJ) [Single side]

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



PD and ID Table

Pin	Pin	Acc	sess Tin	ne
Name	No.	60ns	70ns	80ns
PD1	79	Н	H	Н
PD2	163	L	L	L
PD3	80	I	Η	H
PD4	164	L	L	L
PD5	81	L	٦	L
PD6	165	Н	٦	Н
PD7	82	Н	H	L
PD8	166	Н	H	Н
I D0	83	GND	GND	GND
I D1	167	GND	GND	GND

Note) H: VOH, L: VOL

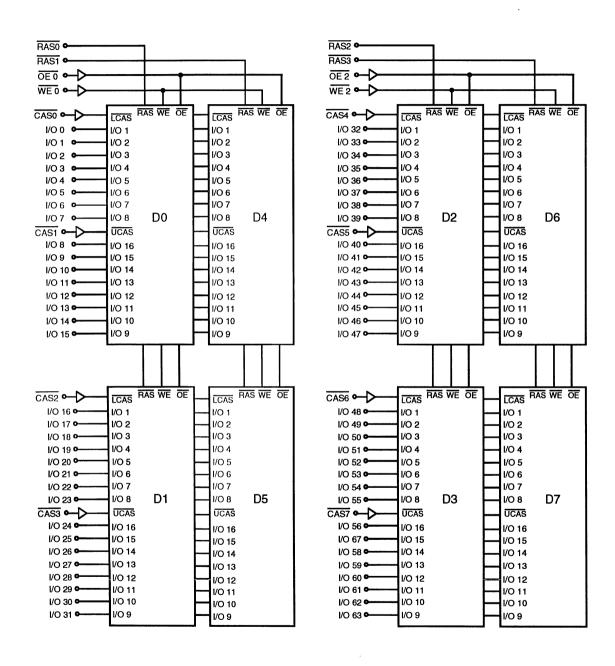
A0 - A9 , B0 : Address Inputs I/O 0-I/O 63 : Data Inputs / Outputs PASO-PAS3 : Row Address Strobe CASO-CAS7 : Column Address Strobe

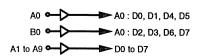
WEO.WE2 : Write Enable
OEO,OE2 : Output Enable
PDE : Presence Detect Enable

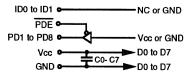
PD1- PD8 : Presence Detect Pins ID0,ID1 : Identity pins

Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram







ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply voltage	VCC		-1.0 to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		10	W
Operating temperature	Topt		0 to +70	C
Storage temperature	Tstg		-55 to +125	$^{\circ}$

Remark

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES:1,2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High level input voltage	VIH		2.4		Vcc + 1.0	V
Low level input voltage	VIL		-1.0		+0.8	v
Ambient temperature	Ta		0		70	C

CAPACITANCE (Ta=25 $^{\circ}$ C, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 - A9, B0			20	pF
	C I 2	WE 0, WE 2	-		20	pF
	C I 3	RAS 0 - RAS 3			45	pF
	C I 4	CAS 0 - CAS 7			20	pF
	C I 5	OE 0, OE 2			20	pF
Data Input/ Output capacitance	C I/O	I/O 0 - I/O 63			20	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	Iccl	RAS, CAS Cycling	trac=60ns		712 672	mA	3, 4, 7
		trc=trc (MIN.) , IO=0mA	trac=80ns		632		
Standby Current	Icc2	\overline{RAS} , $\overline{CAS} \ge V_{IH(MIN)}$ \overline{RAS} , $\overline{CAS} \ge V_{CC}$ -0.2V			80	mA	
					72		
RAS only refresh current	Icc3	RAS Cycling, CAS ≥ V _{IH}	trac=60ns		712	mA	
			trac=70ns		672		3, 4, 7
		trc=trc(min.), IO=0mA	trac=80ns		632		
Operating Current (Fast Page Mode)	Icc4	RAS ≤ VIL, CAS Cycling	trac=60ns		432	mA	
			trac=70ns		392		3, 4, 6
		tPC=tPC MIN., IO=0mA	trac=80ns		352		
CAS before RAS		trc=trc (MIN.)	trac=60ns		712		
	Icc5	ì í	trac=70ns		672	mA	3, 4
refresh current		IO=0mA	trac=80ns		632		
Input Leakage Current	II(L)	VI=0 to 5.5V	RAS -10		+10		
		all other pins not under test = 0V	others	-5	μA		
Output Leakage Current	Io(L)	Outputs are disabled (Hi - Z)		-10	+10	μА	
		VO=0 to 5.5V					
High level output voltage	Von	IO=-5mA		2.4		V	
Low level output voltage	Voi.	IO=+4.2mA			0.4	v	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

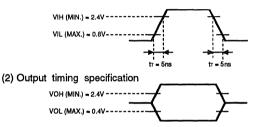
	SYMBOL	tRAC = 60ns		trac = 70ns		trac = 80ns		ивит	NOTES
PARAMETER		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	NOTES
Random Read or Write Cycle Time	tRC	110	-	130	-	150	-	ns	
Read Modify Write Cycle Time	tRWC	173		195	_	215		ns	
Fast Page Mode Cycle Time (Read or Write)	tPC	40	-	45	_	50	_	ns	
Read Modify Write Cycle Time (Fast Page Mode)	tPRWC	85	-	90	-	105	_	ns	
Access Time from RAS	tRAC	-	60	-	70	-	80	ns	10, 11
Access Time from CAS	tCAC	-	20	-	25	-	25	ns	10, 11
Access Time from Column Address	tAA	-	35	-	40	-	45	ns	10, 11
Access Time from CAS Precharge	tACP	_	40	-	45	-	50	ns	11
Access Time from OE	tOEA	-	20	-	25	-	25	ns	11
RAS to Column Address Delay Time	tRAD	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tCLZ	0	-	()	-	0	-	ns	11
OE to Data Setup Time	tOLZ	0	-	()		0	_	ns	11
Output Buffer Turn-off Delay Time(CAS)	tOFF	0	1.3	()	15	0	15	ns	12
OE to Data Delay Time	tOED	13	-	15	-	15		ns	
Output Buffer Turn-off Delay Time(OE)	tOEZ	0	13	0	15	0	15	ns	12
OE Command Hold Time	tOEH	0	-	0	-	0	_	ns	
OE to RAS inactive Setup Time	tOES	0	-	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	3	50	3	50	3	50	ns	
RAS Precharge Time	tRP	40_	_	50	-	60		ns	
RAS Pulse Width(Random Read, Write Cycle)	tRAS	60	10 000	70	10 000	80	10 000	ns	
RAS Pulse Width (Fast Page Mode)	tRASP	60	125 000	70	125 000	80	125 000	ns	
RAS Hold Time	tRSH	15	-	18	-	20	-	ns	
CAS Pulse Width	tCAS	15	10 000	20	10 000	20	10 000	ns	
CAS Hold Time	tCSH	60	-	70	-	80	-	ns	
RAS to CAS Delay Time	tRCD	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tCRP	5	-	5	-	5		ns	13
CAS Precharge Time	tCPN	10		10	_	10	_	ns	
CAS Precharge Time(Fast Page Mode)	tCP	10	-	10	-	10	-	ns	
RAS Precharge CAS Hold Time	tRPC	5	-	5		5		ns	
RAS Hold Time from CAS Precharge	tRHCP	40	-	45	-	50	-	ns	
Row Address Set Up Time	tASR	5	-	5	-	5	· -	ns	
Row Address Hold Time	tRAH	10		10	-	12		ns	
Column Address Set Up Time	tASC	0		0	-	0	-	ns	
Column Address Hold Time	tCAH	15_		15	-	15		ns	
Column Address Lead Time Referenced to RAS	tRAL	30		35	-	40		ns	
Lead Command Setup Time	tRCS	0		0_		0	_	ns	
Read Command Hold Time Referenced to RAS	tRRH	0		0_	-	0		ns	14
Read Command Hold Time Referenced to CAS	tRCH	0		0		0		ns	14
Write Command Hold Time Referenced to CAS	tWCH	10	<u> </u>	10	-]	15		ns	15

(2)

DAD AMETER	SAMBOL	trac = 60ns		trac = 70ns		trac = 80ns		LIMIT	NOTES
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		NOTES
Write Comand Set-Up Time	tWP	10	-	10	_	15		ms	15
Data-in Seup Time	tDS	0	-	0	_	0	_	ns	16
Data-in Hold Time	tDH	10	-	15	-	15		ns	16
Write Comand Setup Time	tWCS	0		0		0		ns	17
CAS to WE Delay Time	tCWD	38		40		45		ns	17
RAS to WE Delay Time	tRWD	93	-	105		115		ns	17
CAS Precharge Delay Time Referenced to WE (Fast Page Mode)	tCPWD	60	-	65	_	70	-	ns	17
Column Address Delay Time Referenced to WE	tAWD	58		65	-	70	_	ns	17
Write Command Lead Time Referenced to RAS	tRWL	25	-	25	-	25		ns	
Write Command Lead Time Referenced to CAS	tCWL	15	-	15	-	15		ns	
CAS Setup Time for CAS before RAS Refresh	tCSR	5	-	5		5		ns	
CAS Hold Time for CAS before RAS Refresh	tCHR	10	-	10		10		ns	
WE Hold Time	tWHR	15		15]	15		ns	
Refresh Time	tREF	-	16	-	16	-	16	ms	

Notes:

- 1. All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight CAS before RAS or RAS
 only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tac and tec).
- 4. Specified values are obtained with outputs unloaded.
- 5. lcc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- 7. lcc₁ and lcc₃ are measured assuming that address can be changed once or less during RAS ≦VILIMAX.) and CAS ≧VILIMIN.).
- 8. AC measurements assume tr =5ns.
- 9. AC Characteristics test condition
 - (1) Input timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \le t_{RAD(MAX.)}$ and $t_{RCD} \le t_{RCD(MAX.)}$	trac(max.)	TRAC(MAX.)
trad > trad(max.) and tred ≤ tred(max.)	taa(max.)	trad + taa(max.)
trcd > trcd(max.)	tcac(max.)	trod + tcac(max.)

tradimax.) and tradimax.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trad. taa or toac) is to be used for finding out when output data will be available. Therefore, the input conditions trad≥tradimax.) and trad≥tradimax.) will not cause any operation problems.

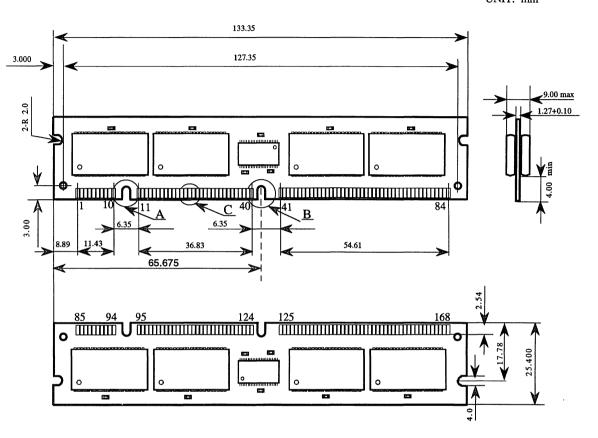
- 11. Loading conditions are 1 TTLs and 100 pF.
- 12. toff (MAX) defines the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp(MIN.) requirement should be applied to RAS / CAS cycles.
- 14. Either trch(MIN.) or trrh(MIN.) should be met in read cycles.
- 15. twp(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, two+(MIN.) should be met.
- 16. tos(MIN.) and toh(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the WE falling edge.
- 17. If twos≧twos (MIN.), the cycle is an early write cycle and the data out will remain Hi Z through the entire cycle. If trwo≧trwo (MIN.), tcwo≧tcwo (MIN.), tawo≥tawo (MIN.) and tcpwo≥ tcpwo (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

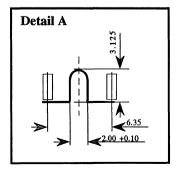
Timing Chart

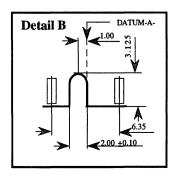
Please refer to Timing Chart 8, page 443.

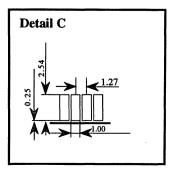
Package Drawing

UNIT: mm









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-		



MC-422000AB72F

2 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-422000AB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μ PD4217800 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- · 2,097,152 words by 72 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time (MIN.)		consumption MAX.)
(MAX.)	(IVIIIV.)	Active	Standby	
MC-422000AB72-60	60 ns	110 ns	5.53 W	
MC-422000AB72-70	70 ns	130 ns	5.06 W	383 mW (CMOS level input)
MC-422000AB72-80	80 ns	150 ns	4.59 W	(CINOS level Input)

- · 2,048 refresh cycles/32 ms
- · CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

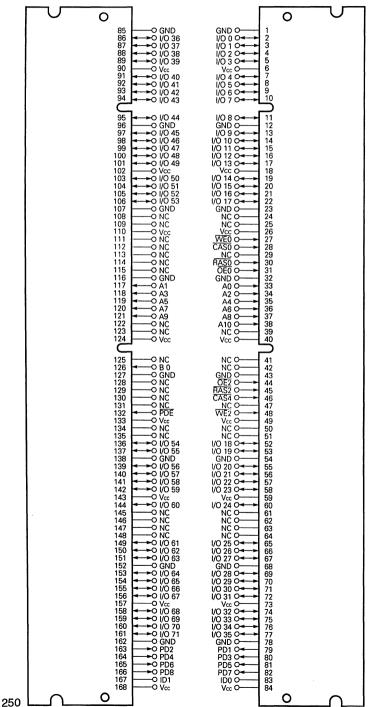
Part number	Access time (MAX.)	Package	Mounted devices
MC-422000AB72F-60	60 ns	168-pin Dual In-line Memory Module	9 pieces of μPD4217800G5
MC-422000AB72F-70	70 ns	(Socket Type)	(400 mil TSOP(II))
MC-422000AB72F-80	80 ns	Edge connector: Gold plating	[Double side]

The information in this document is subject to change without notice.



Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Ad	Access Time				
Name	No.	60 ns	70 ns	80 ns			
PD1	79	Н	Н	Н			
PD2	163	L	L	L			
PD3	80	L	L	L			
PD4	164	Н	Н	Н			
PD5	81	L	L	L			
PD6	165	Н	L	Н			
PD7	82	Н	н	L			
PD8	166	L	L	L			
ID0	83	GND	GND	GND			
ID1	167	GND	GND	GND			

Remark H: Voh, L: Vol

A0 - A10, B0 : Address Inputs

I/O 0 - I/O 71 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

CAS0, CAS4 : Column Address Strobe

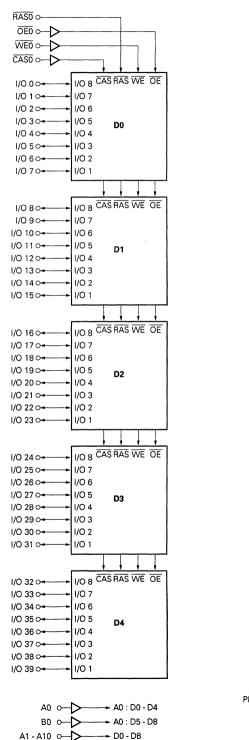
WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

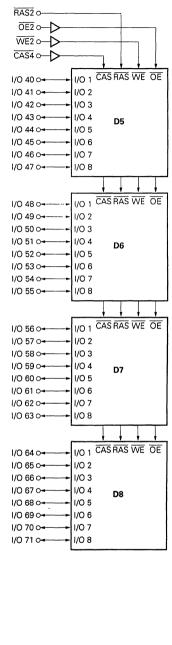
PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

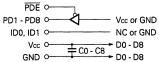
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection



Block Diagram









Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-1.0 to +7.0	٧
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Рь		11 .	W
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	.c

Capacitance (TA = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cn	A0 - A10, B0			20	рF
	C12	WEO, WE2			20	
	Сіз	RASO, RAS2			50	
	C14	CASO, CAS4			20	
	C ₁₅	OE0, OE2			20	
Data Input/Output capacitance	Ci/o	I/O0 - I/O71			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc (MIN.) lo = 0 mA	TRAC	= 60 ns = 70 ns = 80 ns		1,054 964 874	mA	3, 4, 7
Standby current	Icc2	\overline{RAS} , $\overline{CAS} \ge V_{IH (MIN.)}$ \overline{RAS} , $\overline{CAS} \ge V_{CC} - 0.2 \text{ V}$		0 mA 0 mA		82 73	mA	
RAS only refresh current	lcc3	RAS Cycling CAS ≥ ViH (MIN.) trc = trc (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns		1,054 964 874	mA	3, 4, 5, 7
Operating current (Fast page mode)	Icc4	$\overline{RAS} \le V_{IL \; (MAX.)}, \; \overline{CAS} \; Cycling$ $t_{PC} = t_{PC \; (MIN.)}$ $t_{PC} = 0 \; mA$	trac	= 60 ns = 70 ns = 80 ns		694 604 514	mA	3, 4, 6
CAS before RAS refresh current	lcc5	RAS Cycling trc = trc (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns	-	,1,054 964 874	mA	3, 4
Input leakage current	lı (L)	V ₁ = 0 to 5.5 V All other pins not under test	= 0 V	RAS Others	-10 -5	+10	μА	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)			-10	+10	μА	
High level output voltage	Vон	lo = -5.0 mA			2.4		٧	
Low level output voltage	Vol	lo = +4.2 mA				0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

	I	trac	= 60 ns	trac	= 70 ns	TRAC	= 80 ns		T
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Read Modify Write Cycle Time	tawc	173		195		215		ns	
Fast Page Mode Cycle Time	tec	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	terwo	85		90		100		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		20		23		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	TACP		40		45		50	ns	11
Access Time from OE	toea		20		23		25	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcız	0		0		0		ns	11
OE to Data Setup Time	tolz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
OE to Data Delay Time	toed	13		15		15		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	13	0	15	0	15	ns	12
OE Hold Time	toen	0		0		0		ns	
OE Lead Time Referenced to RAS	tors	0		0		0		ns	
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	tar	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	TRASP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tasa	15		18		20	_	ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tcsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	5		5		5		ns	
RAS Hold Time from CAS Precharge	truce	40		45		50		ns	
Row Address Setup Time	tasr	5		5		5		ns	
Row Address Hold Time	tran	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcan	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

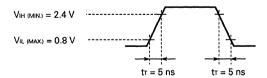


Parameter	Symbol	trac =	= 60 ns	trac =	= 70 ns	trac =	= 80 ns	Unit	Notes
raiametei	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Onit	Notes
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	38		43		45		ns	17
RAS to WE Delay Time	trwo	93		105		115		ns	17
CAS Precharge to WE Delay Time	tcpwb	58		65		70		ns	17
Column Address to WE Delay Time	tawd	58		65		70		ns	17
WE Lead Time Referenced to RAS	trwL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tсня	10		10		10		ns	
WE Setup Time	twsn	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	TREF		32		32		32	ms	

Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t\tau = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (MAX.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

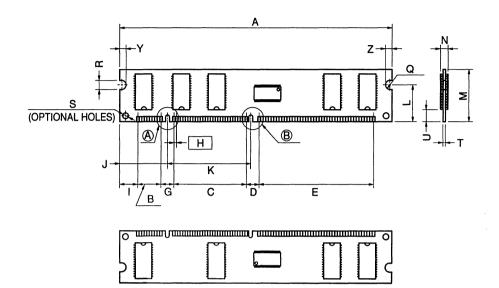
- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to Voh or Vol.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
- 17. If twos ≥ twos (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwo ≥ trwo (MIN.), tcwo ≥ tcwo (MIN.), tawo ≥ tawo (MIN.) and tcrwo ≥ tcrwo (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

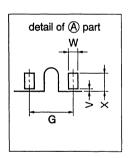
Timing Chart

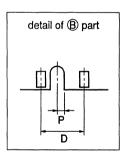
Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
1	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
М	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	φ3.0	φ0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
w	1.0±0.05	0.039 +0.003
X	2.54	0.100
Υ	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A6



MOS INTEGRATED CIRCUIT MC-422000LAB72F

3.3 V OPERATION 2 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-422000LAB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μ PD4217800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 72 bits organization
- · Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	1	consumption MAX.)
·	(IVIAX.)	(IVIIIV.)	Active	Standby
MC-422000LAB72-A60	60 ns	110 ns	3.28 W	
MC-422000LAB72-A70	70 ns	130 ns	2.95 W	147.6 mW (CMOS level input)
MC-422000LAB72-A80	80 ns	150 ns	2.63 W	(Cinico lever input)

- · 2,048 refresh cycles/32 ms
- · CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

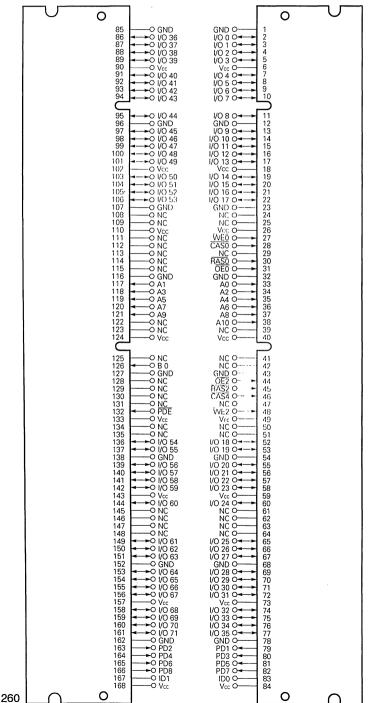
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000LAB72F-A60	60 ns	168-pin Dual In-line Memory Module	9 pieces of μPD4217800LG5
MC-422000LAB72F-A70	70 ns	(Socket Type)	(400 mil TSOP(II))
MC-422000LAB72F-A80	80 ns	Edge connector: Gold plating	[Double side]

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Pin Access Time					
Name	No.	60 ns	70 ns	80 ns			
PD1	79	Η	Н	Н			
PD2	163	L	L	L			
PD3	80	L	L	L			
PD4	164	Н	Н	Н			
PD5	81	L	L	L			
PD6	165	Н	L	Н			
PD7	82	Н	Н	L			
PD8	166	L	L	L			
ID0	83	GND	GND	GND			
ID1	167	GND	GND	GND			

Remark H: Voh, L: Vol

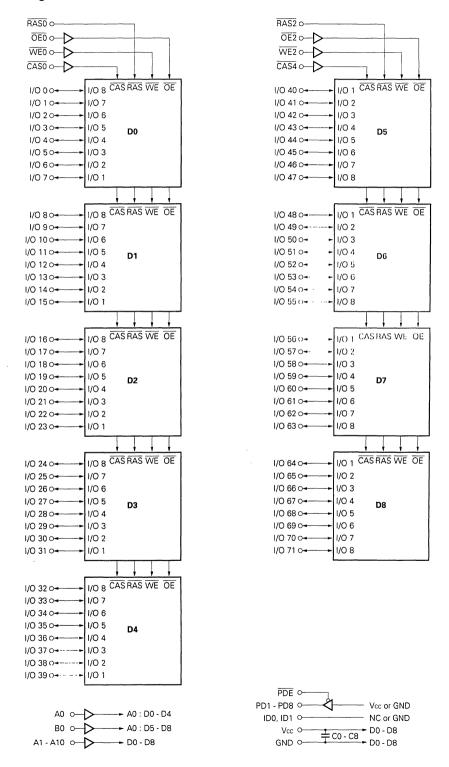
WE0, WE2 : Write Enable OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection



Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-0.5 to +4.6	V
Supply voltage	Vcc		-0.5 to +4.6	V
Output current	lo		20	mA
Power dissipation	Po		11	w
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	٧
High level input voltage	Vih		2.0		Vcc + 0.3	٧
Low level input voltage	VIL		-0.3		+0.8	٧
Operating ambient temperature	TA		0		70	,C

Capacitance ($T_A = 25$ °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A10, B0			20	рF
	Cı2	WEO, WE2			20	
	C13	RASO, RAS2			50	
	Ci4	CASO, CAS4			20	
	C ₁₅	OE0, OE2			20	
Data Input/Output capacitance	Ci/o	I/O0 - I/O71			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling	-	= 60 ns		910	mA	3, 4, 7
		lo = 0 mA	TRAC	= 70 ns		820	1	
		10 = 0 111/1	TRAC	= 80 ns		730		
Standby current	Icc2	RAS, CAS ≥ Vih (MIN.)	lo=	0 mA		82	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo =	0 mA		41		
RAS only refresh current	Іссз	RAS Cycling	TRAC	= 60 ns		910	mA	3, 4, 5, 7
		CAS ≥ Vih (MIN.) trc = trc (MIN.)	trac	= 70 ns		820		
		lo = 0 mA	TRAC	= 80 ns		730		
Operating current	Icc4	$\overline{RAS} \leq Vil.(MAX.), \ \overline{CAS} \ Cycling$	VIL (MAX.), CAS Cycling trac = 60 ns			640	mA	3, 4, 6
(Fast page mode)		1		trac = 70 ns		550		
		lo = 0 mA	TRAC	= 80 ns		460		
CAS before RAS	Icc5	RAS Cycling	TRAC	= 60 ns		910	mA	3, 4
refresh current		trc = trc (MIN.)	trac = 70 ns			820		
		Io = 0 mA	trac	= 80 ns		730		!
Input leakage current	li (L)	Vi = 0 to 3.6 V		RAS	-5	+5	μА	
		All other pins not under test	All other pins not under test = 0 V Others		-5	+1		
Output leakage current	lo (L)	Vo = 0 to 3.6 V Output is disabled (Hi-Z)			- 5	+5	μА	
High level output voltage	Vон	lo = -2.0 mA			2.4		V	
Low level output voltage	Vol	lo = +2.0 mA				0.4	V	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

		TRAC	trac = 60 ns trac = 70 ns		TRAC	= 80 ns		Nata	
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Read Modify Write Cycle Time	trwc	173		195		215		ns	
Fast Page Mode Cycle Time	trc	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t PRWC	85		90		100		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		20		23		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	tacp		40		45		50	ns	11
Access Time from OE	toea		20		23		25	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tclz	0		0		0		ns	11
OE to Data Setup Time	tolz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	13	0	15	0	15	ns	12
OE to Data Delay Time	toed	13		15		15		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	13	0	15	0	15	ns	12
OE Hold Time	toen	0		0		0		ns	
OE Lead Time Referenced to RAS	toes	0		0		0		ns	
Transition Time (Rise and Fall)	t⊤	3	50	3	50	3	50	ns	
RAS Precharge Time	t RP	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	trsh	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	45	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	TRPC	5		5		5		ns	
RAS Hold Time from CAS Precharge	TRHCP	40		45		50		ns	
Row Address Setup Time	tasa	5		5		5		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tсан	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twcн	10		10		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

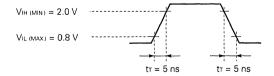


Parameter	Symbol	trac :	= 60 ns	trac =	= 70 ns	trac :	= 80 ns	Unit	Notes
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Onit	Notes
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	38		43		45		ns	17
RAS to WE Delay Time	trwo	93		105		115		ns	17
CAS Precharge to WE Delay Time	tcpwb	58		65		70		ns	17
Column Address to WE Delay Time	tawd	58		65		70		ns	17
WE Lead Time Referenced to RAS	trwL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsr	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
WE Setup Time	twsr	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	tref		32		32		32	ms	

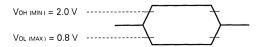
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (trc and tpc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t\tau = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Input Conditions Access Time			
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)		
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (Max.)	trad + taa (MAX)		
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)		

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

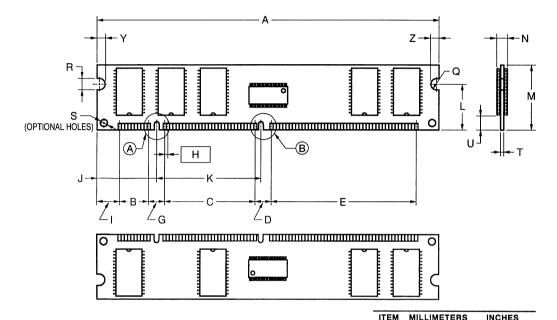
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the WE falling edge.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwb ≥ trwb (MIN.), tcwb ≥ tcwb (MIN.), tawb ≥ tawb (MIN.) and tcrwb ≥ tcrwb (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

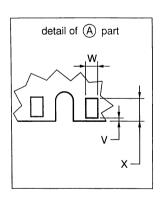
Timing Chart

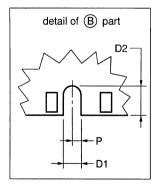
Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







HEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
1	8.89	0.350
J	23.50	0.925
K	43.18	1.70
L	17.78	0.700
М	25.4±0.13	1.000±0.006
N	4.0 MAX.	0.158 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	ϕ 3.0	φ0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
٧	0.25 MAX.	0.010 MAX.
w	1.0±0.05	0.039+0.003
X	2.54±0.10	0.100±0.004
Υ	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A8



MC-424000AB72F

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000AB72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μ PD4217400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- · Fast access and cycle time

Family	Access time R/W cycle time (MAX.) (MIN.)		ſ	consumption MAX.)
	(WAX.)	(WINA.)	Active	Standby
MC-424000AB72-60	60 ns	110 ns	10.73 W	
MC-424000AB72-70	70 ns	130 ns	9.79 W	430 mW (CMOS level input)
MC-424000AB72-80	80 ns	150 ns	8.84 W	(CINICO level Iliput)

- · 2,048 refresh cycles/32 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

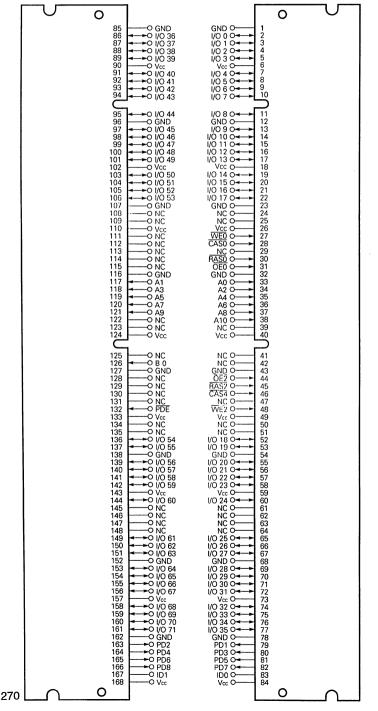
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AB72F-60	60 ns	168-pin Dual In-line Memory Module	18 pieces of μPD4217400G3
MC-424000AB72F-70	70 ns	(Socket Type)	(300 mil TSOP(II))
MC-424000AB72F-80	80 ns	Edge connector: Gold plating	[Double side]

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Access Time					
Name	No.	60 ns	70 ns	80 ns			
PD1	79	Н	Н	Н			
PD2	163	Н	Н	Н			
PD3	80	L	L	L			
PD4	164	Н	Н	Н			
PD5	81	L	L	L			
PD6	165	Н	L	Н			
PD7	82	Н	Н	L			
PD8	166	L	L	L			
ID0	83	GND	GND	GND			
ID1	167	GND	GND	GND			

Remark H: Voh, L: Vol

A0 - A10, B0 : Address Inputs

I/O 0 - I/O 71 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

CAS0, CAS4 : Column Address Strobe

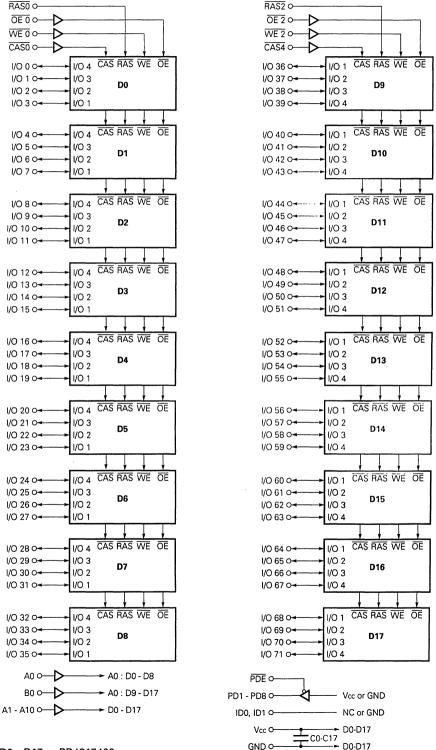
WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection



Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	lo		50	mA
Power dissipation	Ро		20	w
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	Vih		2.4		Vcc + 1.0	٧
Low level input voltage	VıL	,	-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	.c

Capacitance (TA = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A10, B0			20	pF
	Cı2	WE0, WE2			20	
	Сіз	RASO, RAS2			78	
	Ci4	CASO, CAS4			20	
	C ₁₅	OE0, OE2			20	
Data Input/Output capacitance	Ci/o	I/O0 - I/O71			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	Icc1	RAS, CAS Cycling trc = trc (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns		2,044 1,864 1,684	mA	3, 4, 7
Standby current	Icc2	RAS, CAS ≥ VIH (MIN.) RAS, CAS ≥ Vcc - 0.2 V		0 mA 0 mA		100 82	mA	
RAS only refresh current	Icc3	RAS Cycling CAS ≥ Vir (MIN.) trc = trc (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns		2,044 1,864 1,684	mA	3, 4, 5, 7
Operating current (Fast page mode)	Icc4	RAS VIL (MAX.), CAS Cycling tpc = tpc (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns		1,324 1,144 964	mA	3, 4, 6
CAS before RAS refresh current	Icc5	RAS Cycling trc = trc (MIN.) lo = 0 mA	trac	= 60 ns = 70 ns = 80 ns	***************************************	2,044 1,864 1,684	mA	3, 4
Input leakage current	lı (L)	V _I = 0 to 5.5 V All other pins not under test	= 0 V	RAS Others	-10 -5	+10	μА	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)		-10	+10	μА		
High level output voltage Low level output voltage	Voн Vol	lo = -5.0 mA lo = +4.2 mA			2.4	0.4	V V	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

_		trac = 60 ns		trac = 70 ns		trac = 80 ns			Ī
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Read Modify Write Cycle Time	trwc	175		195		220		ns	
Fast Page Mode Cycle Time	tec	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	tprwc	85		90		105		ns	
Access Time from RAS	TRAC		60	,	70		80	ns	10, 11
Access Time from CAS	tcac		20		23		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	TACP		40		45		50	ns	11
Access Time from OE	toea		20		23		25	ns	11
RAS to Column Address Delay Time	TRAD	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLz	0		0		0		ns	11
OE to Data Setup Time	touz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
OE to Data Delay Time	toed	15		15		20		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	15	0	15	0	20	ns	12
OE Hold Time	toen	0		0		0		ns	
OE Lead Time Referenced to RAS	toes	0		0		0		ns	
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	tap	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	TRASP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	trsh	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tcsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	trpc	5		5		5		ns	
RAS Hold Time from CAS Precharge	TRHCP	40		45		50		ns	
Row Address Setup Time	tasr	5		5		5		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	15		15		15		ns	
Column Address Lead Time Referenced to RAS	TRAL	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	terh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

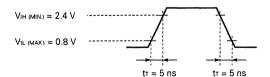


Parameter	Symbol	trac = 60 ns		trac = 70 ns		trac = 80 ns		Unit	Notes
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Onit	Notes
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	40		43		50		ns	17
RAS to WE Delay Time	trwo	95		105		120		ns	17
CAS Precharge to WE Delay Time	tcpwd	58		65		70		ns	17
Column Address to WE Delay Time	tawd	60		65		75		ns	17
WE Lead Time Referenced to RAS	trwL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tcha	10		10		10		ns	
WE Setup Time	twsr	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	TREF		32		32		32	ms	

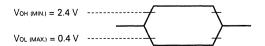
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ ViL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t\tau = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification





10. For read cycles, access time is defined as follows:

Input Conditions	Input Conditions Access Time			
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)		
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	TAA (MAX.)	trad + taa (max.)		
trcd > trcd (MAX.)	TCAC (MAX.)	trcd + tcac (MAX.)		

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

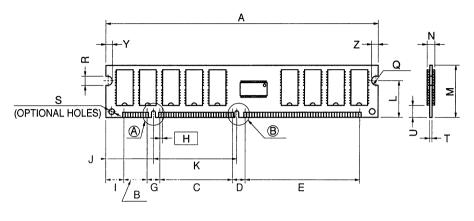
- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
- 17. If twcs ≥ twcs (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If tRWD ≥ tRWD (MIN.), tcWD ≥ tcWD (MIN.), tAWD ≥ tAWD (MIN.) and tcPWD ≥ tcPWD (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

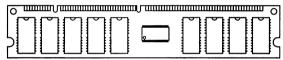
Timing Chart

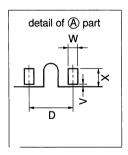
Please refer to Timing Chart 7, page 429.

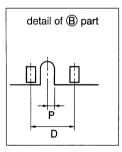
Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)









ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
Е	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
1	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
М	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	φ3.0	φ0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
Χ	2.54 MIN.	0.100 MIN.
Υ	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2



MOS INTEGRATED CIRCUIT MC-424000AC72F

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000AC72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μ PD4216400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- · Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AC72-60	60 ns	110 ns	8.84 W	
MC-424000AC72-70	70 ns	130 ns	7.90 W	430 mW (CMOS level input)
MC-424000AC72-80	80 ns	150 ns	6.95 W	_ (Civios level input)

- · 4,096 refresh cycles/64 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

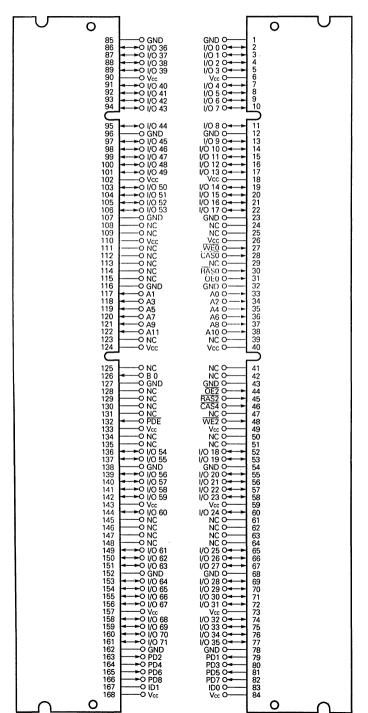
Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AC72F-60	60 ns	168-pin Dual In-line Memory Module	18 pieces of μPD4216400G3
MC-424000AC72F-70	70 ns	(Socket Type)	(300 mil TSOP(II))
MC-424000AC72F-80	80 ns	Edge connector: Gold plating	[Double side]

The information in this document is subject to change without notice.

(Japan)

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD1	79	Н	Н	Н		
PD2	163	Н	H	Н		
PD3	80	L	L	L		
PD4	164	Н	Н	Н		
PD5	81	L	L	L		
PD6	165	Н	L	Н		
PD7	82	Н	Н	L		
PD8	166	L	٦	L		
ID0	83	GND	GND	GND		
ID1	167	GND	GND	GND		

Remark H: Voh, L: Vol

A0 - A11, B0 : Address Inputs

I/O 0 - I/O 71 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

CAS0, CAS4 : Column Address Strobe

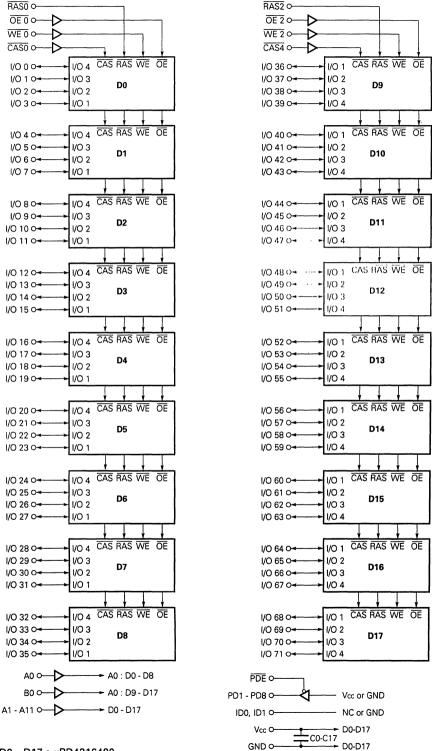
WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection



Block Diagram



Remark D0 - D17 : μPD4216400



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	VT		-1.0 to +7.0	٧
Supply voltage	Vcc		-1.0 to +7.0	٧
Output current	lo		50	mA
Power dissipation	Рь		. 20	w
Operating ambient temperature	TA		0 to +70	°C
Storage temperature	Tstg		-55 to +125	· °C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cıı	A0 - A11, B0			20	
	C12	WEO, WE2			20	
	C13	RASO, RAS2			78	pF
	C14	CASO, CAS4			20	
	C ₁₅	OE0, OE2			20	
Data Input/Output capacitance	Ciro	I/O0 - I/O71			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	Icc1	1.1.1.6, 67.1.6 67.0.1.1.g		= 60 ns		1,684	mA	3, 4, 7
		lo = 0 mA					mA	3, 4, /
			TRAC	= 80 ns		1,324		
Standby current	Icc2	RAS, CAS ≥ VIH (MIN.)		= 0 mA		100	mA	
		RAS, CAS ≥ Vcc - 0.2 V	lo =	= 0 mA		82		
RAS only refresh current	lcc3	Iccs RAS Cycling 1		= 60 ns		1,684		
		CAS ≥ Vih (MIN.)	trac	= 70 ns		1,504	mA	3, 4, 5, 7
				trac = 80 ns		1,324		
Operating current	Icc4	RAS ≤ VIL (MAX.), CAS Cycling		= 60 ns		1,324		
(Fast page mode)		tpc = tpc (MIN.)	trac = 70 ns			1,144	mA	3, 4, 6
		lo = 0 mA	trac	= 80 ns		964		
CAS before RAS	Iccs	RAS Cycling	TRAC	:		1,684		
refresh current		trc = trc (MIN.)	tii∧c ≔ 70 ns			1,504	mA	3, 4
		lo = 0 mA	tnac	: 1 80 ns		1,324		
Input leakage current	lı (L)	Vi = 0 to 5.5 V		RAS	-10	+10	•	
		All other pins not under test	⊔ 0 V	Others	-5	+1	μΑ	
Output leakage current	lo (L)	Vo = 0 to 5.5 V Output is disabled (Hi-Z)			-10	+10	μΑ	
High level output voltage	Vон	lo = -5.0 mA			2.4		٧	
Low level output voltage	Vol	lo = +4.2 mA				0.4	٧	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

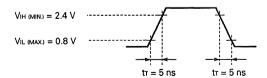
		TRAC	= 60 ns	trac = 70 ns		TRAC	= 80 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Read Modify Write Cycle Time	trwc	175		195		220		ns	
Fast Page Mode Cycle Time	tPC	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t PRWC	85		90		105		ns	
Access Time from RAS	TRAC		60		70		80	ns	10, 11
Access Time from CAS	tcac		20		23		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	TACP		40		45		50	ns	11
Access Time from OE	toea		20		23		25	ns	11
RAS to Column Address Delay Time	TRAD	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcLz	0		0		0		ns	11
OE to Data Setup Time	torz	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	toff	0	15	0	15	0	20	ns	12
OE to Data Delay Time	toed	15		15		20		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	15	0	15	0	20	ns	12
OE Hold Time	toen	0		0		0		ns	
OE Lead Time Referenced to RAS	toes	0		0		0		ns	
Transition Time (Rise and Fall)	tτ	3	50	3	50	3	50	ns	
RAS Precharge Time	trp	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	TRASP	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	trsh	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tсsн	60		70		80		ns	
RAS to CAS Delay Time	trco	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	tcpn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcp	10		10		10		ns	
RAS Precharge CAS Hold Time	TRPC	5		5		5		ns	
RAS Hold Time from CAS Precharge	trhcp	40		45		50		ns	
Row Address Setup Time	tasr	5		5		5		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

Parameter	Symbol	trac =	= 60 ns	trac =	= 70 ns	trac :	= 80 ns	Unit	Notes
Farameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Onit	ivoles
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	40		43		50		ns	17
RAS to WE Delay Time	trwo	95		105		120		ns	17
CAS Precharge to WE Delay Time	tcpwd	58		65		70		ns	17
Column Address to WE Delay Time	tawd	60		65		75		ns	17
WE Lead Time Referenced to RAS	trwL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsr	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
WE Setup Time	twsR	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	t REF		64		64		64	ms	

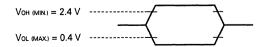
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. lcc1, lcc3, lcc4 and lcc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Iccs is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume $t_T = 5$ ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification





10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (MAX.)	trad + taa (MAX.)
trcd > trcd (MAX.)	tcac (MAX.)	trod + toac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad \geq trad (MAX.) and trad \geq trad (MAX.) will not cause any operation problems.

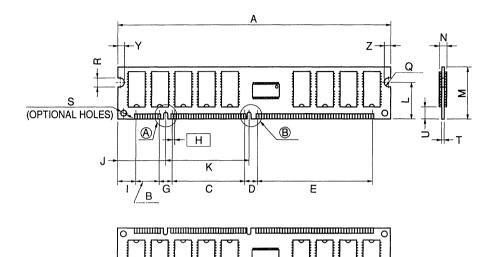
- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the WE falling edge.
- 17. If twos ≥ twos (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwb ≥ trwb (MIN.), tcwb ≥ tcwb (MIN.), tawb ≥ tawb (MIN.) and tcpwb ≥ tcpwb (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

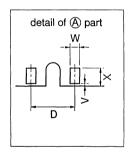
Timing Chart

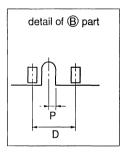
Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
ı	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
М	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
Х	2.54 MIN.	0.100 MIN.
Υ	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2



MC-424000LAB72F

3.3 V OPERATION 4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000LAB72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μ PD4217400L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- · 4,194,304 words by 72 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time	l .	consumption MAX.)
,	(MAX.)	(MIN.)	Active	Standby
MC-424000LAB72-A60	60 ns	110 ns	6.52 W	
MC-424000LAB72-A70	70 ns	130 ns	5.87 W	180 mW (CMOS level input)
MC-424000LAB72-A80	80 ns	150 ns	5.22 W	Civico level ilipati

- · 2,048 refresh cycles/32 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

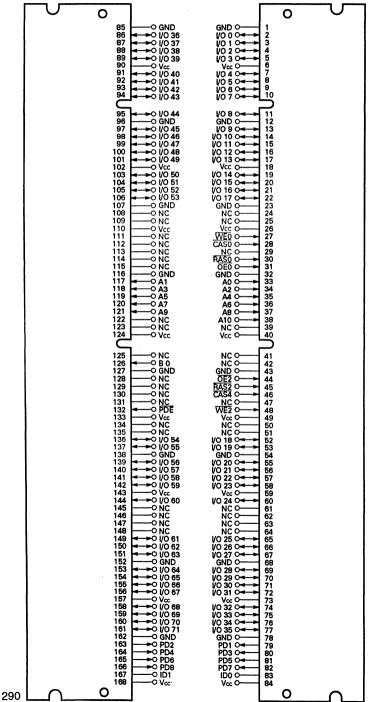
Part number	Access time (MAX.)	Package	Mounted devices
MC-424000LAB72F-A60	60 ns	168-pin Dual In-line Memory Module	18 pieces of μPD4217400LG3
MC-424000LAB72F-A70	70 ns	(Socket Type)	(300 mil TSOP(II))
MC-424000LAB72F-A80	80 ns	Edge connector: Gold plating	[Double side]

The information in this document is subject to change without notice.

M10520EJ5V0DS00 (Japan) 289

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Access Time				
Name	No.	60 ns	70 ns	80 ns		
PD1	79	Н	Н	Н		
PD2	163	Н	H	H		
PD3	80	L	L	L		
PD4	164	Н	Н	Н		
PD5	81	L	L	L		
PD6	165	Н	L	Н		
PD7	82	Н	Н	L		
PD8	166	L	L	L		
ID0	83	GND	GND	GND		
ID1	167	GND	GND	GND		

Remark H: Voh, L: Vol

A0 - A10, B0 : Address Inputs

I/O 0 - I/O 71 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

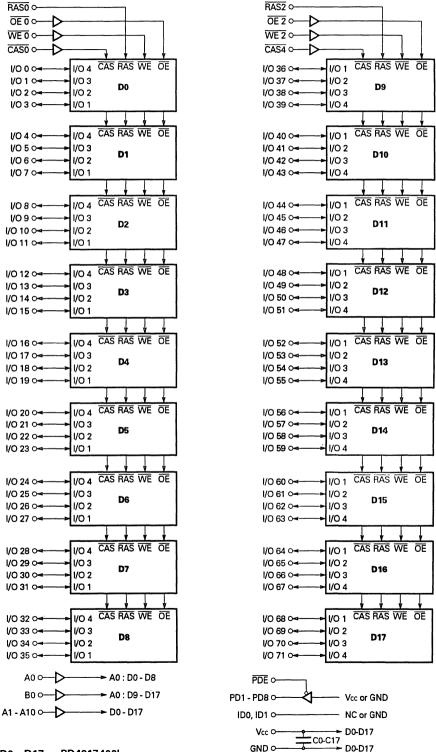
CAS0, CAS4 : Column Address Strobe

WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

IDO, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-0.5 to +4.6	V
Supply voltage	Vcc		-0.5 to +4.6	٧
Output current	lo		20	mA
Power dissipation	P₀	1	20	w
Operating ambient temperature	TA		0 to +70	·c
Storage temperature	Tstg		-55 to +125	·c

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	٧
High level input voltage	ViH		2.0		Vcc + 0.3	٧
Low level input voltage	VIL		-0.3		+0.8	٧
Operating ambient temperature	TA		0		70	•c

Capacitance (TA = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{l1}	A0 - A10, B0		:	20	pF
	C ₂	WEO, WE2			20	
	C ₃	RASO, RAS2			78	
	C 4	CASO, CAS4			20	
	Сњ	OE0, OE2			20	
Data Input/Output capacitance	Cvo	I/O0 - I/O71			20	рF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	_		MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc (MIN.) lo = 0 mA	trac =	60 ns 70 ns 80 ns		1,810	mA	3, 4, 7
Standby current	lcc2	RAS, CAS ≥ Vih (MIN.) RAS, CAS ≥ Vcc – 0.2 V	lo = 0	mA		1,450 100 50	mA	
RAS only refresh current	lcc3	RAS Cycling CAS ≥ ViH (MIN.) trc = trc (MIN.) lo = 0 mA	trac =	60 ns 70 ns		1,810 1,630	mA	3, 4, 5, 7
Operating current (Fast page mode)	Icc4	RAS \leq VIL (MAX.), CAS Cycling trc = trc (MIN.) lo = 0 mA	trac =	60 ns 70 ns 80 ns		1,270 1,090 910	mA	3, 4, 6
CAS before RAS refresh current	lccs	RAS Cycling trc = trc (MIN.) lo = 0 mA	truc =	60 ns 70 ns 80 ns		1,810 1,630 1,450	mA	3, 4
Input leakage current	lı (L)	V _I = 0 to 3.6 V RAS All other pins not under test = 0 V Others		-6 -5	+6	μА		
Output leakage current	lo (L)	Vo = 0 to 3.6 V Output is disabled (Hi-Z)			-5	+5	μА	
High level output voltage Low level output voltage	Voh Vol	lo = -2.0 mA			2.4	0.4	V V	



AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

		trac	= 60 ns	trac	= 70 ns	trac	= 80 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read/Write Cycle Time	trc	110		130		150		ns	
Read Modify Write Cycle Time	trwc	175		195		220		ns	
Fast Page Mode Cycle Time	tec	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	terwo	85		90		105		ns	
Access Time from RAS	trac		60		70		80	ns	10, 11
Access Time from CAS	tcac		20		23		25	ns	10, 11
Access Time Column Address	taa		35		40		45	ns	10, 11
Access Time from CAS Precharge	tacp		40		45		50	ns	11
Access Time from OE	toea		15		18		20	ns	11
RAS to Column Address Delay Time	trad	15	30	15	35	17	40	ns	10
CAS to Data Setup Time	tcız	0		0		0		ns	11
OE to Data Setup Time	toız	0		0		0		ns	11
Output Buffer Turn-off Delay Time from CAS	torr	0	15	0	15	0	20	ns	12
OE to Data Delay Time	toed	15		15		20		ns	
Output Buffer Turn-off Delay Time from OE	toez	0	15	0	15	0	20	ns	12
OE Hold Time	t oeh	0		0		0		ns	
OE Lead Time Referenced to RAS	toes	0		0		0		ns	
Transition Time (Rise and Fall)	tт	3	50	3	50	3	50	ns	
RAS Precharge Time	tnr	40		50		60		ns	
RAS Pulse Width	tras	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	trasp	60	125,000	70	125,000	80	125,000	ns	
RAS Hold Time	tren	15		18		20		ns	
CAS Pulse Width	tcas	15	10,000	18	10,000	20	10,000	ns	
CAS Hold Time	tсвн	60		70		80		ns	
RAS to CAS Delay Time	trcp	20	40	20	50	25	60	ns	10
CAS to RAS Precharge Time	tcrp	5		5		5		ns	13
CAS Precharge Time	topn	10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	tcr	10		10		10		ns	
RAS Precharge CAS Hold Time	trec	5		5		5		ns	
RAS Hold Time from CAS Precharge	TRHCP	40		45		50		ns	
Row Address Setup Time	tasn	5		5		5		ns	
Row Address Hold Time	trah	10		10		12		ns	
Column Address Setup Time	tasc	0		0		0		ns	
Column Address Hold Time	tcah	15		15		15		ns	
Column Address Lead Time Referenced to RAS	tral	30		35		40		ns	
Read Command Setup Time	trcs	0		0		0		ns	
Read Command Hold Time Referenced to RAS	trrh	0		0		0		ns	14
Read Command Hold Time Referenced to CAS	trch	0		0		0		ns	14
WE Hold Time Referenced to CAS	twch	10		10		15		ns	15
WE Pulse Width	twp	10		10		15		ns	15

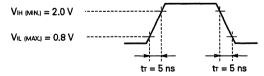


Parameter	Symbol	trac =	= 60 ns	trac :	= 70 ns	trac :	= 80 ns	Unit	Nana
rarameter	Symbol	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Omit	Notes
Data-in Setup Time	tos	0		0		0		ns	16
Data-in Hold Time	tон	10		15		15		ns	16
Write Command Setup Time	twcs	0		0		0		ns	17
CAS to WE Delay Time	tcwp	40		43		50		ns	17
RAS to WE Delay Time	trwo	95		105		120		ns	17
CAS Precharge to WE Delay Time	tcrwo	58		65		70		ns	17
Column Address to WE Delay Time	tawd	60		65		75		ns	17
WE Lead Time Referenced to RAS	TRWL	25		25		25		ns	
WE Lead Time Referenced to CAS	tcwL	15		15		15		ns	
CAS Setup Time (CAS before RAS Refresh)	tcsn	5		5		5		ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10		10		ns	
WE Setup Time	twsn	10		10		10		ns	
WE Hold Time	twnr	15		15		15		ns	
Refresh Time	tref		32		32		32	ms	

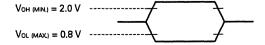
Notes

- 1. All voltages are referenced to GND.
- 2. After power up, wait more than 100 μ s and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.
- 3. Icc1, Icc3, Icc4 and Icc5 depend on cycle rates (tRc and tPc).
- 4. Specified values are obtained with outputs unloaded.
- 5. Icc3 is measured assuming that all column address inputs are held at either high or low.
- 6. lcc4 is measured assuming that all column address inputs are switched only once during each fast page cycle.
- Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VIL (MAX.) and CAS ≥ VIH (MIN.).
- 8. AC measurements assume tr = 5 ns.
- 9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification





10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and tred ≤ tred (MAX.)	TRAC (MAX.)	trac (MAX.)
trad > trad (MAX.) and tred ≤ tred (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trod + toac (MAX.)

trad (MAX.) and trad (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad (MAX.) and trad ≥ trad (MAX.) will not cause any operation problems.

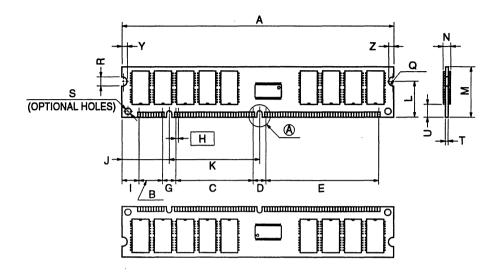
- 11. Loading conditions are 1 TTL and 100 pF.
- 12. toff (MAX.) and toez (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to VoH or VoL.
- 13. tcrp (MIN.) requirements should be applied to RAS/CAS cycles.
- 14. Either trch (MIN.) or trrh (MIN.) should be met in read cycles.
- 15. twp (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twch (MIN.) should be met.
- 16. tos (MIN.) and toh (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.
- 17. If twos ≥ twos (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwo ≥ trwo (MIN.), tcwo ≥ tcwo (MIN.), tawo ≥ tawo (MIN.) and tcrwo ≥ tcrwo (MIN.), the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

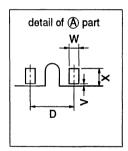
Timing Chart

Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
ı	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
М	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A3

8 Byte DIMM [Hyper Page (EDO)]





MOS INTEGRATED CIRCUIT MC-421000FA64FB

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE HYPER PAGE MODE

Description

The MC-421000FA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μ PD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 64 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time	Hyper page mode cycle Time		onsumption IAX.)
	(MAX.) (MIN.)		(MIN.)	Active	Standby
MC-421000FA64-60	60 ns	104 ns	25 ns	3.89 W	336 mW
MC-421000FA64-70	70 ns	124 ns	30 ns	3.68 W	(CMOS level input)

- 1,024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

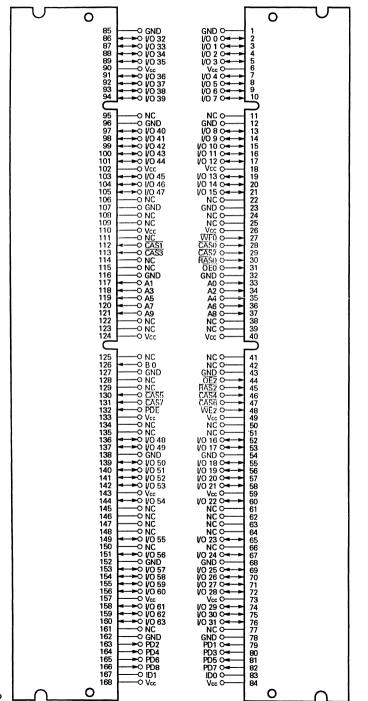
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000FA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type)	4 pieces of μPD4218165LE
MC-421000FA64FB-70	70 ns	Edge connector: Gold plating	(400 mil SOJ) [Single side]

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Acces	s Time
Name	No.	60 ns	70 ns
PD1	79	L	L
PD2	163	L	L
PD3	80	Н	Н
PD4	164	L	L
PD5	81	H	н
PD6	165	Н	L
PD7	82	H	н
PD8	166	Н	Н
ID0	83	GND	GND
ID1	167	GND	GND

Remark H: Voh, L: Vol

A0 - A9, B0 : Address Inputs

I/O 0 - I/O 63 : Data Inputs/Outputs

RAS0, RAS2 : Row Address Strobe

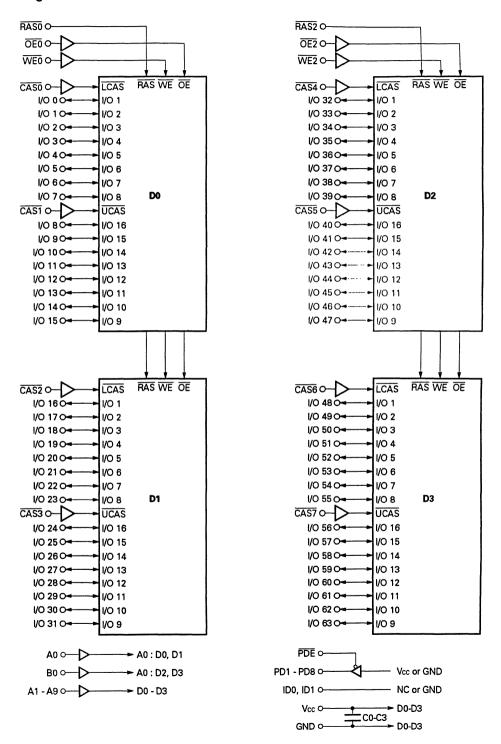
CAS0 - CAS7 : Column Address Strobe

WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram





Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-1.0 to +7.0	٧
Supply voltage	Vcc		-1.0 to +7.0	٧
Output current	lo		50	mA
Power dissipation	Po		6	W
Operating ambient temperature	TA		0 to +70	·c
Storage temperature	Tstg		-55 to +125	·c

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	ViH		2.4		Vcc + 1.0	٧
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	·c

Capacitance (TA = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Clı	A0 - A9, B0			20	pF
•	C ₂	WEO, WE2			20	
	C _l 3	RASO, RAS2			45	
	C ₁₄	CASO - CAS7			20	
	Св	OE0, OE2			20	
Data Input/Output capacitance	Cvo	1/00 - 1/063			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	current Icc1 RAS, CAS Cycling trac = 60 trac = 70 trac = 70		trac =	60 ns		700	mA	1,2,3
			70 ns		660		.,-,-	
Standby current	lcc2	RAS, CAS ≧ VIH (MIN.), Io = 0 mA	RAS, CAS ≧ Vih (MIN.), lo = 0 mA			68		
otaliaby ourient	1002	RAS, CAS ≧ Vcc - 0.2 V, lo = 0	RAS, CAS ≧ Vcc – 0.2 V, lo = 0 mA			64	mA	
		RAS Cycling CAS ≧ Viн (мім.)	trac = 60 ns			700		4004
RAS only refresh current	Іссз	trc = trc (MIN.) lo = 0 mA				660	mA ,	1,2,3,4
Operating current		RAS ≦ VIL (MAX.) CAS Cycling	trac = 60 ns			500	mA	405
(Hyper page mode)	Icc4	thpc = thpc (MIN.) lo = 0 mA				460	IIIA	1,2,5
CAS before RAS	lcc5	RAS Cycling trc = trc (MIN.)	t rac :::	60 ns		700	mA	1,2
refresh current		lo = 0 mA	trac = 70 ns			660	IIIA	1,2
Input leakage current	lı (L)	V _I = 0 to 5.5 V		RAS	-10	+10	μА	
		all other pins not under test = 0	V 	others	-5	+1		
Output leakage current	lo (L)	Vo = 0 to 5.5 V			-10	+10	μА	
		Output is disabled (Hi-Z)						
High level output voltageLow		lo = -2.5 mA			2.4		V	
level output voltage	Vol	lo = +2.1 mA	lo = +2.1 mA			0.4	٧	

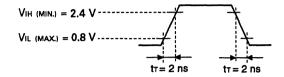
Notes 1. lcc1, lcc3, lcc4, lcc5 depend on cycle rates (tRc and tHPC).

- 2. Specified values are obtained with outputs unloaded.
- 3. Icc1 and Icc3 are measured assuming that address can be changed once or less during $\overline{RAS} \le V_{IL(MAX.)}$ and $\overline{CAS} \ge V_{IH(MIN.)}$.
- 4. Iccs is measured assuming that all column address inputs are held at either high or low.
- 5. lcc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification

(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write Cycle

Parameter	Symbol	trac =	60 ns	trac = 70 ns		Unit	Notes
rarameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	trc	104	_	124	_	ns-	
RAS Precharge Time	t RP	40	_	50	_	ns	
CAS Precharge Time	tcpn	10	_	10		ns	
RAS Pulse Width	tras	60	10 000	70	10 000	ns	
CAS Pulse Width	tcas	10	10 000	12	10 000	ns	
RAS Hold Time	trsH	10	_	12	_	ns	
CAS Hold Time	tсsн	40	_	50	_	ns	
RAS to CAS Delay Time	trco	14	45	14	52	ns	1
RAS to Column Address Delay Time	trad	12	30	12	35	ns	1
CAS to RAS Precharge Time	tcrp	5	_	5	_	ns	2
Row Address Setup Time	tasr	5	_	5	_	ns	
Row Address Hold Time	trah	10	_	10	_	ns	
Column Address Setup Time	tasc	0	_	0	_	ns	
Column Address Hold Time	tcah	10	_	12	_	ns	
OE Lead Time Referenced to RAS	toes	0	_	0	_	ns	
CAS to Data Setup Time	tcLZ	0	_	0		ns	
OE to Data Setup Time	toLZ	0	_	0	_	ns	
OE to Data Delay Time	toed	13	_	15	_	ns	
Masked Byte Write Hold Time Referenced to RAS	tmrh	0	_	0	_	ns	
Transition Time (Rise and Fall)	tτ	1	50	1	50	ns	
Refresh Time	tref	_	16	_	16	ms	



Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≦ trad (MAX.) and trcd ≦ trcd (MAX.)	TRAC (MAX.)	trac (MAX.)
trad > trad (MAX.) and trcd ≦ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

tradimax.) and tradimax.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or tcxc) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ tradimax.) and trad ≥ tradimax.) will not cause any operation problems.

2. tcrp(MIN.) requirement is applied to RAS, CAS cycles.

Read Cycle

Notes
Notes
1
1
1
2
2
3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	TRAC (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (MAX.)

trad(MAX.) and trad(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or tax) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad(MAX.) and trac ≥ trad(MAX.) will not cause any operation problems.

- 2. Either trch(MIN.) or trrh(MIN.) should be met in read cycles.
- toez(MAX.) defines the time when the output achieves the condition of Hi-Z and is not refered Voh or Vol.



Write Cycle

Parameter	Symbol trac = 60 ns		trac =	70 ns		Natas	
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
WE Hold Time Referenced to CAS	twcн	10	_	10	_	ns	1
WE Pulse Width	twp	10	_	10	_	ns	1
WE Lead Time Referenced to RAS	trwL	15	_	17	_	ns	
WE Lead Time Referenced to CAS	tcwL	10	_	12		ns	
WE Setup Time	twcs	0	_	0		ns	2
OE Hold Time	toen	0	_	0	_	ns	
Data-in Setup Time	tos	0	_	0		ns	3
Data-in Hold Time	tон	10	_	10		ns	3

- Notes 1. twp(min.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(min.) should be met.
 - 2. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 - 3. tos(MIN.) and toh(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter Sym		trac = 60 ns		trac =	70 ns		
	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Note
Read Modify Write Cycle Time	trwc	133	-	157	_	ns	
RAS to WE Delay Time	trwd	87	_	99	_	ns	1
CAS to WE Delay Time	tcwp	32	_	37	_	ns	1
Column Address to WE Delay Time	tawd	52	_	59	_	ns	1

Note 1. If twcs ≥ twcs(MIN.) the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwo ≥ trwo(MIN.), tcwo ≥ tcwc(MIN.), tawo ≥ tawo(MIN.), and tcpwo ≥ tcpwc(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.



Hyper Page Mode

_		trac =	60 ns	trac =	70 ns	Unit	
Parameter	Symbol	MIN.	MIN. MAX.		MIN. MAX.		Notes
Read / Write Cycle Time	tHPC	25	_	30	_	ns	1
RAS Pulse Width	trasp	60	125 000	70	125 000	ns	
CAS Pulse Width	thcas	10	10 000	12	10 000	ns	
CAS Precharge Time	tcp	10		10	_	ns	
Access Time from CAS Precharge	tacp	_	40		45	ns	
CAS Precharge to WE Delay Time	tcpwd	52	_	59	_	ns	2
RAS Hold Time from CAS Precharge	trhcp	40	_	45		ns	
Read Modify Write Cycle Time	thprwc	66	_	75	_	ns	
Data Output Hold Time	tonc	5	_	5	_	ns	
OE to CAS Hold Time	tосн	5	_	5		ns	
OE Precharge Time	toep	6		5	_	ns	
Output Buffer Turn-off Delay from WE	twez	0	13	0	15	ns	3,4
WE Pulse Width	twpz	10		10	_	ns	4
Output Buffer Turn-off Delay from RAS	tofr	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from CAS	torc	0	13	0	15	ns	3.4

Notes 1. thpc(MIN.) is applied to access time from CAS

- 2. If twos ≥ twos(MIN.), the cycle is an early write cycle and the data out will remain Hi Z through the entire cycle. If trwo ≥ trwo(MIN.), tcwo ≥ tcwo(MIN.), tawo ≥ tawo(MIN.), and tcpwo ≥ tcpwo(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
- 3. tofc(MAX.), tofr(MAX.) and twez(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to VoH or VoL.
- 4. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) RAS, CAS: Inactive (at the end of read cycle)

WE: inactive, OE: active

torc is effective when RAS is inactivated before CAS is inactivated.

toff is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)

WE: inactive, OE: inactive ... toez is effective.

(3) Both RAS and CAS are inactive or RAS is active and CAS is inactive (at the end of read cycle)

WE, OE: active and either tran or tran must be met... twez, twez are effective.

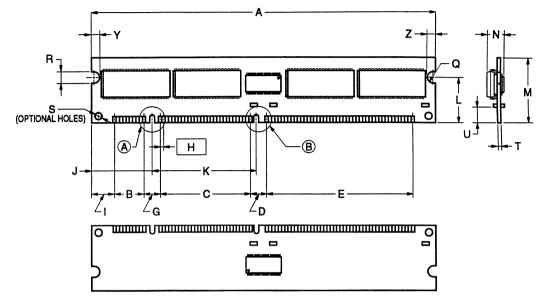
Refresh Cycle

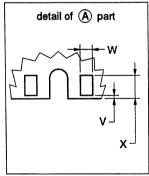
110.10011 0 7 0.10							
		trac = 60 ns		trac =	: 70 ns		
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Note
CAS Setup Time	tcsn	5	_	5	_	ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10	_	10	_	ns	
RAS Precharge CAS Hold Time	trpc	5	-	5	_	ns	
WE Hold Time (Hidden Refresh Cycle)	twnn	15	_	15		ns	

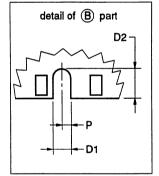
Timing Chart

Please refer to Timing Chart 9, page 457.

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.05 (T.P.)
ı	8.89	0.350
J	23.495	0.925
К	42.18	1.661
L	17.78	0.7000
М	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
w	1.0±0.05	0.039+0.003
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A5



MOS INTEGRATED CIRCUIT MC-422000FA64FB

2 M-WORD BY 64-BIT DYNAMIC RAM MODULE HYPER PAGE MODE

Description

The MC-422000FA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μ PD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- · Hyper page mode (EDO)
- · 2,096,152 words by 64 bits organization
- · Fast access and cycle time

Family	Access time	R/W cycle time	Hyper page mode cycle Time		nsumption AX.)
·	(IVIAA.)	(MIN.)	(MIN.)	Active	Standby
MC-422000FA64-60	60 ns	104 ns	25 ns	3.73 W	357 mW
MC-422000FA64-70	70 ns	124 ns	30 ns	3.52 W	(CMOS level input)

- · 1,024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

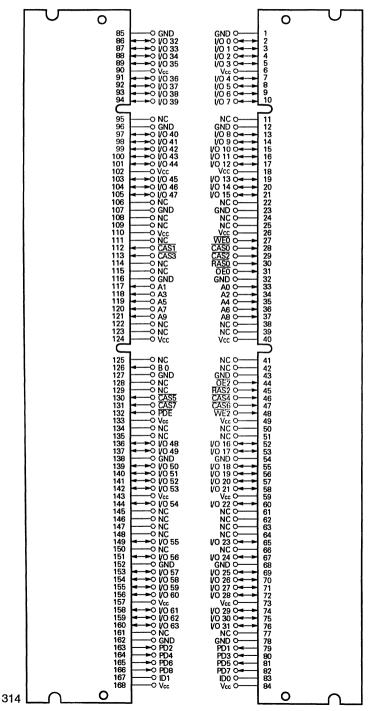
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices	
MC-422000FA64FB-60	60 ns 168-pin Dual In-line Memory Module (Socket Type)		8 pieces of μPD4218165LE	
MC-422000FA64FB-70	70 ns	Edge connector: Gold plating	(400 mil SOJ) [Single side]	

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



PD and ID Table

Pin	Pin	Access Time					
Name	No.	60 ns	70 ns				
PD1	79	Н	Н				
PD2	163	L	L				
PD3	80	н	н				
PD4	164	٦	L				
PD5	81	Н	H				
PD6	165	Η	L				
PD7	82	Н	Н				
PD8	166	Н	Н				
ID0	83	GND	GND				
ID1	167	GND	GND				

Remark H: Voh, L:Vol

A0 - A9, B0 : Address Inputs

1/O 0 - I/O 63 : Data Inputs/Outputs

RAS0 - RAS2 : Row Address Strobe

CAS0 - CAS7 : Column Address Strobe

WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

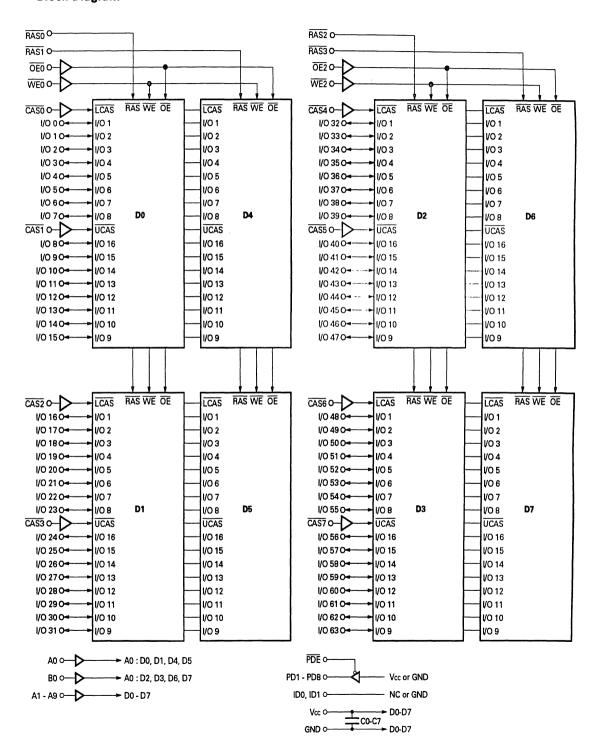
PDE : Presence Detect Enable
PD1 - PD8 : Presence Detect Pins

ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground

NC : No connection



Block Diagram



Remark D0 - D7 : μPD4218165



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	Vτ		-1.0 to +7.0	٧
Supply voltage	Vcc		-1.0 to +7.0	٧
Output current	lo		50	mA
Power dissipation	Po		6	W
Operating ambient temperature	TA		0 to +70	·c
Storage temperature	Tstg		-55 to +125	·c

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		4.75	5.0	5.25	٧
High level input voltage	ViH		2.4		Vcc + 1.0	V
Low level input voltage	VIL		-1.0		+0.8	٧
Operating ambient temperature	TA		0		70	.c

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _l 1	A0 - A9, B0			20	pF
	C ₂	WEO, WE2			20	
	C _{l3}	RAS0 - RAS2			45	
	C _{l4}	CASO - CAS7			20	
	Cis	OE0, OE2			20	
Data Input/Output capacitance	Cvo	I/O0 - I/O63			20	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	lcc1	RAS, CAS Cycling trc = trc(MIN.)	trac = 60 ns			710	mA	1,2,3
		lo = 0 mA	trac≃	70 ns		670	,	1,2,0
Standby current	Icc2	RAS, CAS ≧ VIH (MIN.), Io = 0 mA	•			76	mA.	
otanasy danoni	1002	RAS, CAS ≧ Vcc – 0.2 V, lo = 0 mA		68	mA			
		RAS Cycling CAS ≧ Vih (MIN.)	trac = 60 ns			710	4	1,2,3,4
RAS only refresh current	Іссз	trc = trc (MIN.) lo = 0 mA	trac = 70 ns			670	mA	1,2,3,4
RAS ≦ VIL (MAX.) Operating current CAS Cycling	trac = 60 ns			510	mA	1,2,5		
(Hyper page mode)	Icc4	thpc = thpc (MIN.) lo = 0 mA	trac =	70 ns		470		1,2,5
CAS before RAS	lcc5	RAS Cycling trc = trc (MIN.)	trac=	60 ns		710	mA	12
refresh current		lo = 0 mA	trac =	70 ns		670	IIIA	1,2
Input leakage current	li (L)	Vi = 0 to 5.5 V		RAS	-10	+10	μА	
put roundgo curront	(=,	all other pins not under test = 0	٧	others	5	+1	Ĺ	
Output leakage current	lo (L)	Vo = 0 to 5.5 V		-10	+10	μА		
		Output is disabled (Hi-Z)						
High level output voltageLow	Vон	lo = -2.5 mA			2.4		٧	
level output voltage	Vol	lo = +2.1 mA				0.4	٧	

Notes 1. Icc1, Icc3, Icc4, Icc5 depend on cycle rates (trc and thrc).

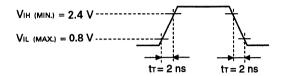
- 2. Specified values are obtained with outputs unloaded.
- 3. Icc1 and Icc3 are measured assuming that address can be changed once or less during RAS ≤ VILIMAX.) and CAS ≥ VIHIMIN.).
- 4. Iccs is measured assuming that all column address inputs are held at either high or low.
- lcc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.



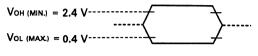
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write Cycle

	S	trac = 60 ns		trac = 70 ns		Unit	
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	tnc	104	_	124	_	ns	
RAS Precharge Time	t RP	40	_	50	_	ns	
CAS Precharge Time	tcpn	10		10	_	ns	
RAS Pulse Width	tras	60	10 000	70	10 000	ns	
CAS Pulse Width	tcas	10	10 000	12	10 000	ns	
RAS Hold Time	trsh	10	_	12	_	ns	
CAS Hold Time	tcsн	40	_	50	_	ns	
RAS to CAS Delay Time	trco	14	45	14	52	ns	1
RAS to Column Address Delay Time	trad	12	30	12	35	ns	1
CAS to RAS Precharge Time	tcrp	5	_	5		ns	2
Row Address Setup Time	tasr	5	_	5	_	ns	
Row Address Hold Time	trah	10	_	10	_	ns	
Column Address Setup Time	tasc	0	. –	0	_	ns	
Column Address Hold Time	tcah	10	_	12	_	ns	
OE Lead Time Referenced to RAS	toes	0	_	0	_	ns	
CAS to Data Setup Time	tclz	0	_	0		ns	
ŌĒ to Data Setup Time	toız	0	_	0		ns	
OE to Data Delay Time	toed	13	_	15	_	ns	
Masked Byte Write Hold Time Referenced to RAS	tmrh	0	_	0	_	ns	
Transition Time (Rise and Fall)	tτ	1	50	1	50	ns	
Refresh Time	tref	_	16	_	16	ms	



Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	trac (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	taa (max.)	trad + taa (max.)
trcd > trcd (MAX.)	TCAC (MAX.)	trcd + tcac (max.)

tradimax.) and tradimax.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, taa or tcac) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≧ tradimax.) and trade tradimax.) will not cause any operation problems.

2. tcrp(MIN.) requirement is applied to RAS, CAS cycles.

Read Cycle

Parameter	Symbol	trac = 60 ns		trac = 70 ns		Unit	Notes
rarameter	Symbol	MIN.	MAX.	MIN.	MAX.		Notes
Access Time from RAS	trac	_	60	_	70	ns	1
Access Time from CAS	tcac	_	20	_	23	ns	1
Access Time from Column Address	taa	_	35	_	40	ns	1
Access Time from OE	toea	_	20	_	23	ns	
Column Address Lead Time Referenced to RAS	tral	30	_	35	_	ns	
Read Command Setup Time	trcs	0	_	0	_	ns	
Read Command Hold Time Referenced to RAS	trrh	0	_	0		ทธ	2
Read Command Hold Time Referenced to CAS	tксн	0	_	0	_	ns	2
Output buffer Turn-off Delay Time from OE	toez	0	13	0	15	ns	3
CAS Hold Time to OE	tсно	5	_	5	_	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
trad ≤ trad (MAX.) and trcd ≤ trcd (MAX.)	TRAC (MAX.)	trac (MAX.)
trad > trad (MAX.) and trcd ≤ trcd (MAX.)	EAA (MAX.)	trad + taa (max.)
trcd > trcd (MAX.)	tcac (MAX.)	trcd + tcac (max.)

trad(MAX.) and trad(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (trac, tax or tcxc) is to be used for finding out when output data will be available. Therefore, the input conditions trad ≥ trad(MAX.) and trad ≥ trad(MAX.) will not cause any operation problems.

- 2. Either trch(MIN.) or trrh(MIN.) should be met in read cycles.
- 3. toez(MAX.) defines the time when the output achieves the condition of Hi-Z and is not refernced VoH or VoL.



Write Cycle

	Symbol	trac = 60 ns		trac = 70 ns			Ninan
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
WE Hold Time Referenced to CAS	twch	10	_	10	-	ns	1
WE Pulse Width	twp	10	_	10	_	ns	1
WE Lead Time Referenced to RAS	trwL	15	-	17	_	ns	
WE Lead Time Referenced to CAS	tcwL	10		12		ns	
WE Setup Time	twcs	, 0		0	_	ns	2
OE Hold Time	tоен	0	_	0	_	ns	
Data-in Setup Time	tos	0	_	0	_	ns	3
Data-in Hold Time	t DH	10	_	10	_	ns	3

- Notes 1. twp(min.) is applied to late write cycles or read modify write cycles. In early write cycles, twch(min.) should be met.
 - 2. If twcs ≥ twcs(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 - 3. tos(MIN.) and toh(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

	Symbol	trac = 60 ns		trac = 70 ns			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Note
Read Modify Write Cycle Time	trwc	133	_	157	_	ns	
RAS to WE Delay Time	trwo	87	_	99	_	ns	1
CAS to WE Delay Time	tcwp	32	_	37	_	ns	1
Column Address to WE Delay Time	tawd	52	_	59	_	ns	1

Note 1. If twcs ≥ twcs(MIN.) the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If trwo ≥ trwo(MIN.), tcwo ≥ tcwo(MIN.), tawo ≥ tawo(MIN.), and tcpwo ≥ tcpwo(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.



Hyper Page Mode

•	0	trac =	60 ns	trac = 70 ns			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Notes
Read / Write Cycle Time	tHPC	25	_	30	_	ns	1
RAS Pulse Width	trasp	60	125 000	70	125 000	ns	
CAS Pulse Width	thcas	10	10 000	12	10 000	ns	
CAS Precharge Time	tcp	10	_	10	_	ns	
Access Time from CAS Precharge	tacp	_	40		45	ns	
CAS Precharge to WE Delay Time	tcpwd	52	_	59	_	ns	2
RAS Hold Time from CAS Precharge	t RHCP	40	-	45	_	ns	
Read Modify Write Cycle Time	tHPRWC	66	_	75	_	ns	
Data Output Hold Time	t DHC	Б	_	5	_	ns	
OE to CAS Hold Time	tосн	Б		5		ns	
OE Precharge Time	toep	5		5	_	ns	
Output Buffer Turn-off Delay from WE	twez	0	13	0	15	ns	3,4
WE Pulse Width	twez	10		10	_	ns	4
Output Buffer Turn-off Delay from RAS	tofr	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from CAS	torc	0	13	0	15	ns	3.4

Notes 1. thec(MIN.) is applied to access time from CAS

- 2. If twos ≥ twos(MIN.), the cycle is an early write cycle and the data out will remain Hi Z through the entire cycle. If trwo ≥ trwo(MIN.), tcwo ≥ tcwo(MIN.), tawo ≥ tawo(MIN.), and tcpwo ≥ tcpwo(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
- 3. tofc(MAX.), toff(MAX.) and twez(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to VoH or VoL.
- 4. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) RAS, CAS: Inactive (at the end of read cycle)

WE: inactive, OE: active

torc is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

toff is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)

WE: inactive, OE: inactive ... to Ez is effective.

(3) Both RAS and CAS are inactive or RAS is active and CAS is inactive (at the end of read cycle)

WE,OE:active and either trrh or trch must be met... twez, twez are effective.

Refresh Cycle

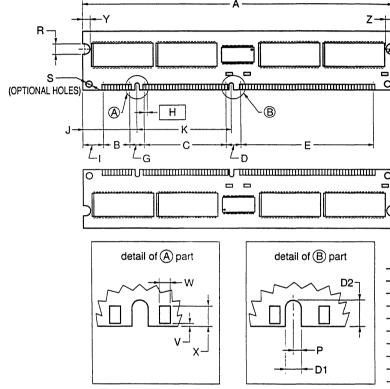
Tierresir Oyure							
		trac = 60 ns		trac = 70 ns			
Parameter	Symbol	MIN.	MAX.	MIN.	MAX.	Unit	Note
CAS Setup Time	tcsr	5	_	5	_	ns	
CAS Hold Time (CAS before RAS Refresh)	tchr	10		10	_	ns	
RAS Precharge CAS Hold Time	trpc	5	_	5	l –	ns	
WE Hold Time (Hidden Refresh Cycle)	twnr	15		15	_	ns	

Timing Chart

Please refer to Timing Chart 9, page 457.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.05 (T.P.)
1	8.89	0.350
J	23.495	0.925
К	42.18	1.661
L	17.78	0.7000
М	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
Р	1.0	0.039
<u> Q</u>	R 2.0	R 0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	ø3.0	¢0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
	0.25 MAX.	0.010 MAX.
w	1.0±0.05	0.039+0.003
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A7



MC-422000FB72F

2M -WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (ECC)

Description

The MC-422000FB72F is a 2 097 152 words by 72 bits dynamic RAM module on which 9 pieces of 16M DRAM (μ PD 4217805) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2 097 152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time	Hyper page mode cycle time (MIN.)	Power cor (MA)	nsumption K.)
(MAX.) (MIN.) cycle		cycle unic (wirt)	Active	Standby	
MC- 422000FB72-60	60 ns	104 ns	25 ns	5.51w	368mw
MC- 422000FB72-70	70 ns	124 ns	30 ns	5.04w	(CMOS level)

- 2 048 refresh cycles/32 ms
- CAS before RAS refresh , RAS only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +5.0 V±0.25V power supply

Ordering information

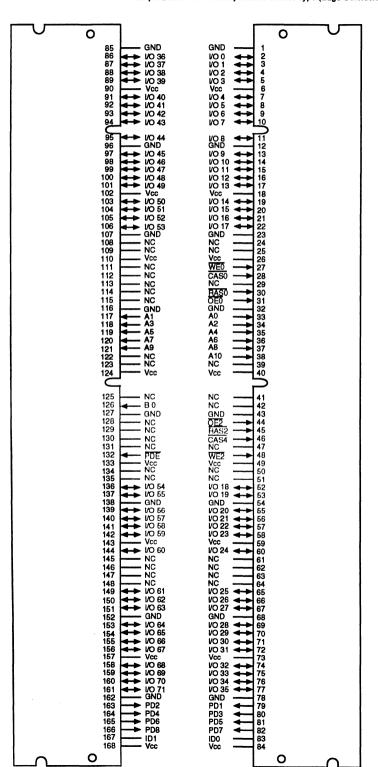
Part Number	Access time (MAX.)	Package	Mounted devices
MC- 422000FB72F-60	60ns	168-pin Dual In-line Memory Module	9 pieces of uPD 4217805G5
MC- 422000FB72F-70	70ns	(Socket Type) Edge connector: Gold plating	(400mil TSOP) [Double side]

The information in this document is subject to change without notice.

M10549EJ1V0DS00 (Japan) 325

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



PD and ID Table

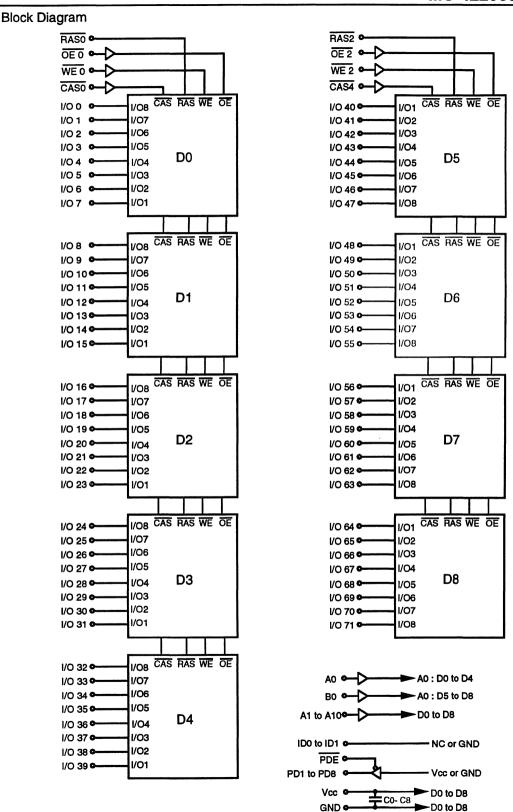
Pin	Pin	Accses	ss Time
Name	No.	60ns	70ns
PD1	79	Н	Н
PD2	163	L	L
PD3	80	L	L
PD4	164	Н	Н
PD5	81	Н	Н
PD6	165	H	L
PD7	82	Н	Н
PD8	166	L	L
I DO	83	GND	GND
I D1	167	GND	GND

Note) H: VOH, L: VOL

A0 - A10, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
RAS0, RAS2 : Row Address Strobe
CAS0, CAS4 : Column Address Strobe
WE0, WE2 : Write Enable

OEO, OE2 : Output Enable
PDE : Presence Detect Enable
PD1- PD8 : Presence Detect Pins

ID0, ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply voltage	Vcc		-1.0 to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		11	W
Operating temperature	Topt		0 to +70	C
Storage temperature	Tstg		-55 to +125	${\mathfrak C}$

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES:1,2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	v
High level input voltage	VIH		2.4		Vcc + 1.0	v
Low level input voltage	VIL		-1.0		+0.8	v
Ambient temperature	Ta		0		70	τ

CAPACITANCE (Ta=25 $^{\circ}$ C, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
	CI1	A0 - A10, B0			20	pF
	CI2	WE 0, WE 2			20	pF
Input capacitance	C I 3	RAS 0, RAS 2			50	pF
	CI4	CAS 0, CAS 4			20	pF
	C15	OE 0, OE 2			20	pF
Data Input/ Output capacitance	C 1/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
		RAS, CAS Cycling	trac=60ns		1 050	mA	2.4.7
Operating Current	Icc1	trc=trc (MIN.) , IO=0mA	trac=70ns		960	ша	3, 4, 7
Standby Current	Icc2	\overline{RAS} , $\overline{CAS} \ge V_{IH(MIN.)}$			90	mA	
Journal Current	1002	\overline{RAS} , $\overline{CAS} \ge Vcc-0.2V$			70	ША	
DAG	Icc3	RAS Cycling, CAS ≥ V _{IH}	trac=60ns		1 050		
RAS only refresh current	1003	trc=trc(min.), IO=0mA	trac=70ns		960	mA	3, 4, 5, 7
Operating Current	Icc4	RAS ≤ VIL, CAS Cycling	trac=60ns		870	A	2.4.6
(Hyper Page Mode)	2001	thpc=thpc (MIN.), IO=0mA	trac=70ns		780	mA	3, 4, 6
CAS before RAS	Icc5	trc=trc (min.)	trac=60ns		1 050	mA	3, 4
refresh current	ICC	IO=0mA	trac=70ns		960	шА	3, 4
Input Leakage Current	I _{I(L)}	VI=0 to 5.25V	RAS	-10	+10		
input Leakage Current	II(L)	all other pins not under test = 0V	others	-5	+1	μА	
O and I ask of Comment		Outputs are disabled (Hi - Z)					
Output Leakage Current	Io(L)	VO=0 to 5.25V		-10	+10	μА	
High level output voltage	Vон	IO=-5.0mA		2.4		V	
Low level output voltage	Vol	IO=+4.2mA			0.4	v	

AC CHARACTERISTICS

Notes 8,9

(Recommended Operating Conditions unless otherwise noted)

(1/2)

		trac = 60ns		trac = 70ns			(1/2
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT	NOTES
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157		ns	
Access Time from RAS	tRAC	-	60		70	ns	10,11
Access Time from CAS	tCAC	_	20	-	23	ns	10,11
Access Time from Column Address	tAA	-	35	-	40	ns	10,11
Access Time from CAS Precharge	tACP	-	40	-	45	ns	11
Access Time from OE	tOEA	-	20	-	23	ns	11
RAS to Column Address Delay Time	tRAD	12	30	12	35	ns	10
CAS to Data Setup Time	tCLZ	0	-	0	-	ns	11
OE to Data Setup Time	tOLZ	0	-	0	-	ns	11
OE to Data Delay Time	tOED	13	-	15	-	ns	
Output Buffer Turn-off Delay Time from OE	tOEZ	0	13	0	15	ns	12
OE Hold Time	tOEH	0	-	0	-	ns	
OE Lead Time Referenced to RAS	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tΤ	1	50	1	50	ns	
RAS Precharge Time	tRP	40	_	50	-	ns	
RAS Pulse Width	tRAS	60	10,000	70	10,000	ns	
RAS Hold Time	tRSH	10	-	12	-	ns	
CAS Pulse Width	1CAS	10	10,000	12	10,000	ns	
CAS Hold Time	1CSH	40	-	50	_	ns	
RAS to CAS Delay Time	tRCD	14	45	14	52	ns	10
CAS to RAS Precharge Time	tCRP	5	_	5	_	ns	13
CAS Precharge Time	tCPN	10	-	10	-	ns	
RAS Precharge CAS Hold Time	tRPC	5	-	5	-	ns	
RAS Hold Time from CAS Precharge	tRHCP	40		45	-	ns	
Row Address Setup Time	tASR	5	_	5	-	ns	
Row Address Hold Time	tRAH	10	_	10	-	ns	
Column Address Setup Time	tASC	0	-	0	-	ns	
Column Address Hold Time	tCAH	10	-	12	_	ns	
Column Address Lead Time Referenced to RAS	tRAL	30	-	35	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to RAS	tRRH	0	-	0	-	ns	14
Read Command Hold Time Referenced to CAS	tRCH	0	-	0	-	ns	14
WE Hold Time Referenced to CAS	tWCH	10		10			15
WE Pulse Width	tWP	10		10	-	ns	15
Data-in Setup Time	tDS	0		0	-	ns	16
Data-in Hold Time	tDH	10		10	-	ns	16
Write command Setup Time	tWCS	0		0	-	ns	17
CAS to WE Delay Time	tCWD	32		37	-	ns	17
RAS to WE Delay Time	tRWD	87		99		ns	17
Column Address to WE Delay Time	tAWD	52	-	59	-	ns	17

(2/2)

DADAMETER	SYMBOL	trac	= 60ns	trac	= 70ns	UNIT	NOTES
PARAMETER	STMBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
WE Lead Time Referenced to RAS	tRWL	15	-	17	-	ns	
WE Lead Time Referenced to CAS	tCWL	10		12		ns	
CAS Setup Time for CAS before RAS Refresh	tCSR	5		5		ns	
CAS Hold Time for CAS before RAS Refresh	tCHR	10		10		ns	
WE Setup Time	tWSR	10	-	10	-	ns	
WE Hold Time	tWHR	15	-	15	-	ns	
Refresh Time	tREF	-	32	-	32	ms	

HYPER PAGE MODE

DADAMETER	SYMBOL	trac = 60ns		trac = 70ns		LINIT	Nome
PARAMETER	SIMBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
Read / Write Cycle Time	tHPC	25	-	30	-	ns	
RAS Pulse Width	tRASP	60	125,000	70	125,000	ns	
CAS Pulse Width	tHCAS	10	10,000	12	10,000	ns	
CAS Precharge Time	tCP	10		10	-	ns	
CAS Precharge to WE Delay Time	tCPWD	52	•	59	,	ns	17
Read Modify Write Cycle Time	tHPRWC	66		75	•	ns	
Data Output Hold Time	tDHC	5	•	5		ns	
OE to CAS Hold Time	tOCH	5	-	5		ns	18
OE Precharge Time	tOEP	5	-	5	-	ns	
CAS Hold Time to OE	tCHO	5	-	5	-	ns	18
Output Buffer Turn-off Delay from WE	tWEZ	0	13	0	15	ns	12, 18
WE Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from RAS	tOFR	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from CAS	tOFC	0	13	0	15	ns	12, 18

- Notes:
 1. All voltages are referenced to GND.
 - 2. After power up, wait more than 100 µs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
 - 3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
 - 4. Specified values are obtained with outputs unloaded.
 - 5. ICC3 is measured assuming that all column address inputs are held at either high or low.
 - 6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
 - 7 ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≦VIL(MAX.) and CAS≧VIH(MIN.).
 - 8. AC measurements assume tT =2ns.

Notes:

- 9. AC Characteristics test condition
 - (1) Input timing specification

(2) Output timing specification

10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
tRAD ≤ tRAD(MAX.) and tRCD ≤ tRCD(MAX.)	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≤ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
tRCD > tRCD(MAX.)	tCAC(MAX.)	tRCD+tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≥tRAD(MAX.) and tRCD≥tRCD(MAX.) will not cause any operation problems.

- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. tOFC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
- 13. tCRP(MIN.) requirement is applied to RAS/CAS cycles preceded by any cycles.
- 14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
- 15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
- 16. tDS(MIN.) and tDH(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the WE falling edge.
- 17. If tWCS≧tWCS (MIN.), the cycle is an early write cycle and the data out will remain Hi Z through the entire cycle. If tRWD≧tRWD (MIN.), tCWD≧tCWD(MIN.), tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell.

 If neither of the above conditions is met, the state of the data out is indeterminate.
- 18. To make I/O to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) RAS, CAS: inactive (at the end of read cycle)

WE: inactive, OE: active

tOFC is effective when RAS is inactivated before CAS is inactivated.

tOFR is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)

WE: active, OE: active...tWEZ, tWPZ are effective.

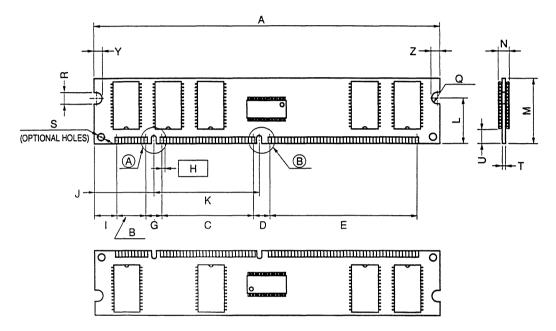
WE: inactive, OE: inactive...tOEZ is effective.

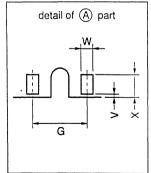
Timing Chart

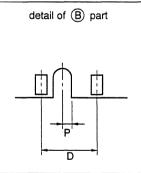
Please refer to Timing Chart 10, page 473.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE) OUTLINE DRAWINGS







ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
1	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
М	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	φ3.0	φ0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
w	1.0±0.05	0.039+0.003
X	2.54	0.100
Υ	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A6



MOS INTEGRATED CIRCUIT MC-422000LFB72F

3.3 V OPERATION 2M -WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (ECC)

Description

The MC-422000LFB72F is a 2 097 152 words by 72 bits dynamic RAM module on which 9 pieces of 16M DRAM (μ PD 4217805L) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2 097 152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power co (MA	nsumption X.)
	(1117-01.)	(IVIIIV.)	Gyolo umo (mirt.)	Active	Standby
MC- 422000LFB72-A60	60 ns	104 ns	25 ns	3.28 w	147.6mw
MC- 422000LFB72-A70	70 ns	124 ns	30 ns	2.95 w	(CMOS level)

- 2 048 refresh cycles/32 ms
- CAS before RAS refresh , RAS only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3 $V \pm 0.3 V$ power supply

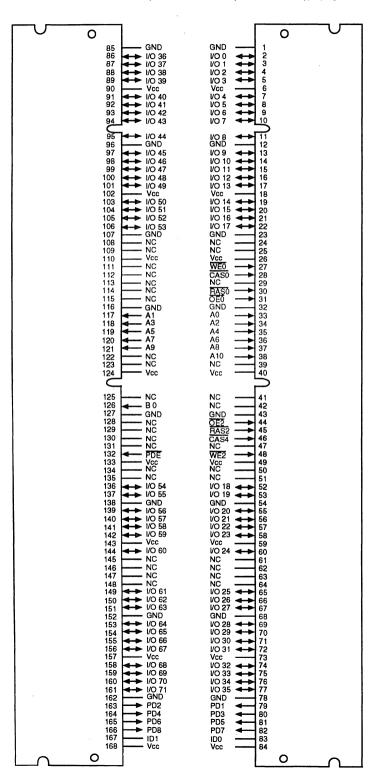
Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 422000LFB72F-A60	60ns	168-pin Dual In-line Memory Module	9 pieces of uPD 4217805LG5
MC- 422000LFB72F-A70	70ns	(Socket Type) Edge connector: Gold plating	(400mil TSOP) [Double side]

The information in this document is subject to change without notice.

110042EJ4V0DS00 (Japan) 335

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



PD and ID Table

Dulla ID Table								
Pin	Pin	Accses	ss Time					
Name	No.	60ns	70ns					
PD1	79	Н	Н					
PD2	163	L	L					
PD3	80	L	L					
PD4	164	Н	Н					
PD5	81	I	Н					
PD6	165	Η	L					
PD7	82	Н	Н					
PD8	166	L	L					
I D0	83	GND	GND					
I D1	167	GND	GND					

Note) H: VOH, L: VOL

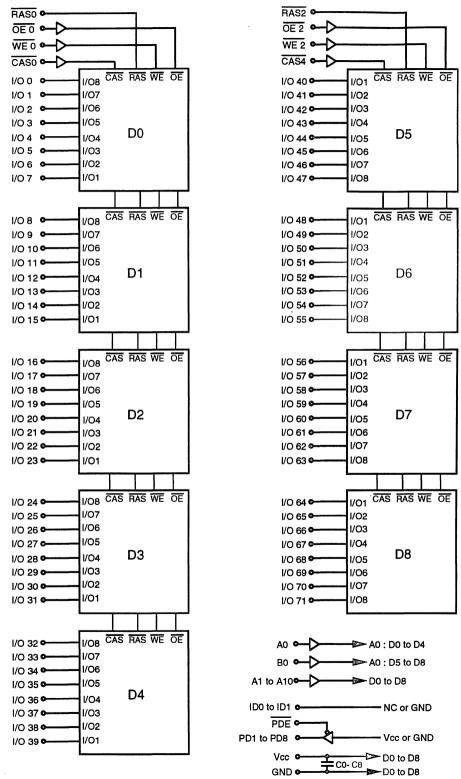
A0 - A10, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
RASO, RAS2 : Row Address Strobe
CASO, CAS4 : Column Address Strobe
WEO WE2 : Write Fnable

WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1- PD8 : Presence Detect Pins

ID0, ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +4.6	V
Supply voltage	VCC		-0.5 to +4.6	V
Output current	IO		20	mA
Power dissipation	PD		11	W
Operating temperature	Topt		0 to +70	С
Storage temperature	Tstg		-55 to +125	ч

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES:1,2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		Vcc + 0.3	v
Low level input voltage	VIL		-0.3		+0.8	v
Ambient temperature	Ta		0		70	${\mathfrak C}$

CAPACITANCE (Ta=25 $^{\circ}$ C, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
	CII	A0 - A10, B0			20	pF
	C 1 2	WE 0, WE 2			20	pF
Input capacitance	C13	RAS 0, RAS 2			50	pF
	C I 4	CAS 0, CAS 4			20	pF
	C 1 5	OE 0, OE 2			20	pF
Data Input/ Output capacitance	C I/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
		RAS, CAS Cycling	trac=60ns		910	mA	2 4 7
Operating Current	Icc1	trc=trc (min.) , IO=0mA	trac=70ns		820	шл	3, 4, 7
Standby Current	Icc2	RAS, CAS ≥ VIH(MIN.)			82	mA	
Standby Current	ICCZ	\overline{RAS} , $\overline{CAS} \ge Vcc-0.2V$			41	IIIA	
DAG	T2	RAS Cycling, CAS ≥ V _{IH}	trac=60ns		910	A	
RAS only refresh current	Icc3	trc=trc(min.), IO=0mA	trac=70ns		820	mA	3, 4, 5, 7
Operating Current	Icc4	RAS ≤ VIL, CAS Cycling	trac=60ns		820	A	0.4.5
(Hyper Page Mode)	1001	thpc=thpc (MIN.), IO=0mA	trac=70ns		730	mA	3, 4, 6
CAS before RAS	Icc5	trc=trc (MIN.)	trac=60ns	91	910	mA	2.4
refresh current	iccs	IO=0mA	trac=70ns		820	III.A	3, 4
Input Leakage Current	Total	VI=0 to 3.6V	RAS	-5	+5		
input Leakage Current	It(L)	all other pins not under test = 0V	others	-5	+1	μА	
O to A Toology Course	_	Outputs are disabled (Hi - Z)			_		
Output Leakage Current	Io(L)	VO=0 to 3.6V		-5	+5	μА	
High level output voltage	Vон	IO=-2.0mA		2.4		v	
Low level output voltage	Vol	IO=+2.0mA			0.4	v	

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

		trac:	= 60ns	trac	= 70ns	LINIT	NOTES
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157	-	ns	
Access Time from RAS	tRAC	_	60	_	70	ns	10,11
Access Time from CAS	tCAC	_	20	-	23	ns	10,11
Access Time from Column Address	tAA	-	35	-	40	ns	10,11
Access Time from CAS Precharge	tACP	-	40	-	45	ns	11
Access Time from OE	tOEA	-	20	-	23	ns	11
RAS to Column Address Delay Time	tRAD	12	30	12	35	ns	10
CAS to Data Setup Time	tCLZ	0	-	0	-	ns	11
OE to Data Setup Time	tOLZ	0	-	0	-	ns	11
OE to Data Delay Time	tOED	13	-	15	-	ns	
Output Buffer Turn-off Delay Time from OE	tOEZ	0	13	0	15	ns	12
OE Hold Time	tOEH	0	-	0	-	ns	
OE Lead Time Referenced to RAS	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tΤ	1	50	1	50	ns	
RAS Precharge Time	tRP	40	-	50	-	ns	
RAS Pulse Width	tRAS	60	10,000	70	10,000	ns	
RAS Hold Time	tRSH	10	-	12	-	ns	***************************************
CAS Pulse Width	tCAS	10	10,000	12	10,000	ns	
CAS Hold Time	tCSH	40		50	_	ns	
RAS to CAS Delay Time	tRCD	14	45	14	52	ns	10
CAS to RAS Precharge Time	tCRP	5	_	5	-	ns	13
CAS Precharge Time	tCPN	10	-	10	-	ns	
RAS Precharge CAS Hold Time	tRPC	5	-	5	-	ns	
RAS Hold Time from CAS Precharge	tRHCP	40	-	45	-	ns	
Row Address Setup Time	tASR	5	-	5	-	ns	
Row Address Hold Time	tRAH	10		10	_	ns	
Column Address Setup Time	tASC	0	_ [0	-	ns	
Column Address Hold Time	tCAH	10	-	12	_	ns	
Column Address Lead Time Referenced to RAS	tRAL	30	-	35	_	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to RAS	tRRH	0	_	0	-	ns	14
Read Command Hold Time Referenced to CAS	tRCH	0	-	0	_	ns	14
WE Hold Time Referenced to CAS	tWCH	10	_	10	_	ns	15
WE Pulse Width	tWP	10	-	10	-	ns	15
Data-in Setup Time	tDS	0		0		ns	16
Data-in Hold Time	tDH	10		10		ns	16
Write command Setup Time	tWCS	0		0	-	ns	17
CAS to WE Delay Time	tCWD	32		37	-	ns	17
RAS to WE Delay Time	tRWD	87	-	99		ns	17
Column Address to WE Delay Time	tAWD	52		59	_	ns	17

(2/2)

PARAMETER	SYMBOL	trac = 60n		trac	= 70ns	LINIET	NOTES
PARAMETER	STMBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
WE Lead Time Referenced to RAS	tRWL	15	-	17		ns	
WE Lead Time Referenced to CAS	tCWL	10	-	12	-	ns	
CAS Setup Time for CAS before RAS Refresh	tCSR	5	-	5	-	ns	
CAS Hold Time for CAS before RAS Refresh	tCHR	10	-	10	•	ns	
WE Setup Time	tWSR	10	-	10	-	ns	
WE Hold Time	tWHR	15	-	15	-	ns	
Refresh Time	tREF	-	32	-	32	ms	

HYPER PAGE MODE

DAR AMERICA	ava mor	trac = 60ns		trac = 70ns			Nomea
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
Read / Write Cycle Time	tHPC	25	-	30	-	ns	
RAS Pulse Width	tRASP	60	125,000	70	125,000	ns	
CAS Pulse Width	tHCAS	10	10,000	12	10,000	ns	
CAS Precharge Time	tCP	10	-	10	-	ns	
CAS Precharge to WE Delay Time	tCPWD	52	-	59	-	ns	17
Read Modify Write Cycle Time	tHPRWC	66	-	75	•	ns	
Data Output Hold Time	tDHC	5	-	5	-	ns	
OE to CAS Hold Time	tOCH	5		5	-	ns	18
OE Precharge Time	tOEP	5	-	5	-	ns	
CAS Hold Time to OE	tCHO	5	-	5	-	ns	18
Output Buffer Turn-off Delay from WE	tWEZ	0	13	0	15	ns	12, 18
WE Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from RAS	tOFR	. 0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from CAS	tOFC	0	13	0	15	ns	12, 18

- Notes:
 1. All voltages are referenced to GND.
 - 2. After power up, wait more than 100 µs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
 - 3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
 - 4. Specified values are obtained with outputs unloaded.
 - 5. ICC3 is measured assuming that all column address inputs are held at either high or low.
 - 6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
 - 7. ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≦VIL(MAX.) and CAS≧VIH(MIN.).
 - 8. AC measurements assume tT =2ns.

Notes:

- 9. AC Characteristics test condition
 - (1) Input timing specification

(2) Output timing specification

10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
tRAD ≤ tRAD(MAX.) and tRCD ≤ tRCD(MAX.)	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≤ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
tRCD > tRCD(MAX.)	tCAC(MAX.)	tRCD + tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≥tRAD(MAX.) and tRCD≥tRCD(MAX.) will not cause any operation problems.

- 11. Loading conditions are 1 TTLs and 100 pF.
- 12. 10FC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
- 13. tCRP(MIN.) requirement is applied to RAS/CAS cycles preceded by any cycles.
- 14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
- 15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
- 16. tDS(MIN.) and tDH(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the WE falling edge.
- 17. If tWCS≧tWCS (MIN.), the cycle is an early write cycle and the data out will remain Hi Z through the entire cycle. If tRWD≧tRWD (MIN.), tCWD≧tCWD(MIN.), tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell.

 If neither of the above conditions is met, the state of the data out is indeterminate.
- 18. To make I/O to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) RAS, CAS: inactive (at the end of read cycle)

WE: inactive, OE: active

tOFC is effective when RAS is inactivated before CAS is inactivated.

tOFR is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)

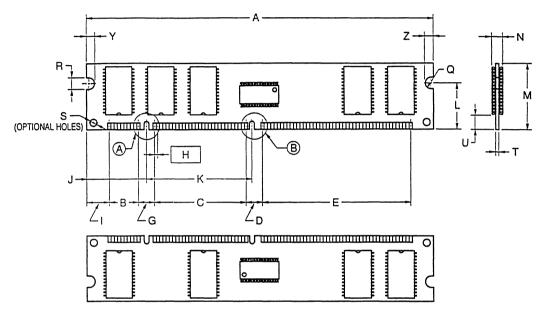
WE: active, OE: active...tWEZ, tWPZ are effective.

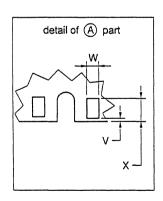
WE: inactive, OE: inactive...tOEZ is effective.

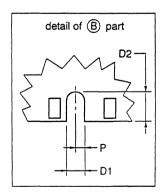
Timing Chart

Please refer to Timing Chart 10, page 473.

Package Drawing







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
- 1	8.89	0.350
J	23.50	0.925
К	43.18	1.70
L	17.78	0.700
М	25.4±0.13	1.000±0.006
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
a	R2.0	R0.079
R	4.0±0.1	0.157+0.005
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039+0.003
×	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A8

PRELIMINARY DATA SHEET



MC-424000FC72F

4M -WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (ECC)

Description

The MC-424000FC72F is a 4 194 304 words by 72 bits dynamic RAM module on which 18 pieces of 16M DRAM (μ PD 4216405) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4 194 304 words by 72 bits organization
- Fast access and cycle time

Family	Access time R/W		Hyper page mode cycle time (MIN.)	Power consumption (MAX.)		
	(1017-174.)	(MIN.)	by old time (wirk:)	Active	Standby	
MC- 424000FC72-60	60 ns	104 ns	25 ns	8.82w	106mw	
MC- 421000FC72-70	70 ns	124 ns	30 ns	7.88w	(CMOS level)	

- 4 096 refresh cycles/64 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +5.5 V±0.25V power supply

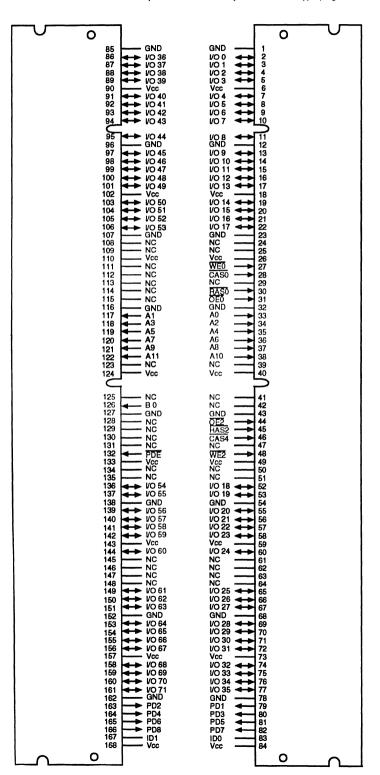
Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 424000FC72F-60	60ns	168-pin Dual In-line Memory Module	18 pieces of uPD 4216405G3
MC- 424000FC72F-70	70ns	(Socket Type) Edge connector: Gold plating	(300mil TSOP) [Double side]

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



PD and ID Table

Pin	Pin Pin		es Time
Name	No.	60ns	70ns
PD1	79	Н	Н
PD2	163	Η	Η
PD3	80	L	L
PD4	164	Н	Н
PD5	81	Н	H
PD6	165	Н	٦
PD7	82	Н	H
PD8	166	L	L
I DO	83	GND	GND
ID1	167	GND	GND

Note) H: VOH, L: VOL

A0 - A11, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
RASO, RAS2 : Row Address Strobe
CASO, CAS4 : Column Address Strobe

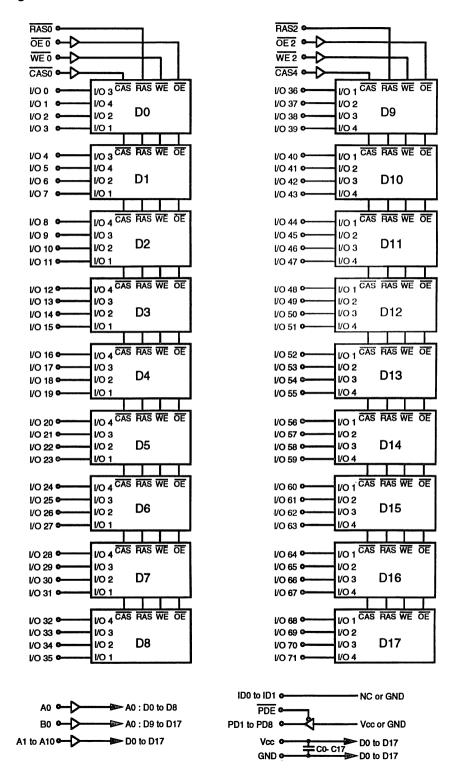
WEO, WE2 : Write Enable
OEO, OE2 : Output Enable
PDE : Presence Detect Enable

PD1- PD8 : Presence Detect Pins
ID0, ID1 : Identity pins
Vcc : Power Supply
GND : Ground

: No connection

NC

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0to +7.0	V
Supply voltage	VCC		-1.0to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		20	W
Operating temperature	Topt		0 to +70	${\mathfrak C}$
Storage temperature	Tstg		-55 to +125	r

Remark

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES:1,2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High level input voltage	VIH		2.4		Vcc + 1.0	v
Low level input voltage	VIL		-1.0		+0.8	V
Ambient temperature	Ta		0		70	r

CAPACITANCE (Ta=25 $^{\circ}$ C , f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 - A10, B0			20	pF
	CI2	WE 0, WE 2			20	pF
	C13	RAS 0, RAS 2			78	pF
	C14	CAS 0, CAS 4			20	pF
!	C15	OE 0, OE 2			20	pF
Data Input/ Output capacitance	C 1/0	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
		RAS, CAS Cycling	trac=60ns		1 680	mA	2.4.7
Operating Current	Icc1	trc=trc (MIN.), IO=0mA	trac=70ns		1 500	шл	3, 4, 7
Standby Current	Icc2	\overline{RAS} , $\overline{CAS} \ge V_{IH(MIN.)}$			100	mA	
Sandy Carrent	1002	\overline{RAS} , $\overline{CAS} \ge Vcc-0.2V$			82	IIIA	
DAC	Icc3	RAS Cycling, CAS ≥ V _{IH}	trac=60ns		1 680		3, 4, 5, 7
RAS only refresh current	1003	trc=trc (MIN.), IO=0mA	trac=70ns		1 500	mA	
Operating Current	Icc4	RAS ≤ VIL, CAS Cycling	trac=60ns		1 680		
(Hyper Page Mode)	1004	thpc=thpc (MIN.), IO=0mA	trac=70ns		1 500	mA	3, 4, 6
CAS before RAS	Icc5	trc=trc (MIN.)	trac=60ns		1 680	mA	2.4
refresh current	ICCS	IO=0mA	trac=70ns		1 500	1117	3, 4
Y Y		VI=0 to 5.25V	RAS	-10	+10		ŧ .
Input Leakage Current	II(L)	all other pins not under test = 0V	others	-5	+1	μА	
	_	Outputs are disabled (Hi - Z)	Outputs are disabled (Hi - Z)				
Output Leakage Current	Io(L)	VO=0 to 5.25V		-10	+10	μА	
High level output voltage	Vон	IO=-5.0mA		2.4		v	
Low level output voltage	Vol	IO=+4.2mA			0.4	v	

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

		trac = 60ns		trac = 70ns		UNIT	NOTES
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.		NOILS
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157	-	ns	
Access Time from RAS	tRAC		60		70	ns	10,11
Access Time from CAS	tCAC	_	20		23	ns	10,11
Access Time from Column Address	tAA	-	35	-	40	ns	10,11
Access Time from CAS Precharge	tACP	-	40	-	45	ns	11
Access Time from OE	tOEA	-	20	-	23	ns	11
RAS to Column Address Delay Time	tRAD	12	30	12	35	ns	10
CAS to Data Setup Time	tCLZ	0	-	0	-	ns	11
OE to Data Setup Time	tOLZ	0	-	0	-	ns	11
OE to Data Delay Time	tOED	13	-	15	-	ns	
Output Buffer Turn-off Delay Time from OE	tOEZ	0	13	0	15	ns	12
OE Hold Time	tOEH	0	-	0	-	ns	
OE Lead Time Referenced to RAS	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tΤ	1	50	• 1	50	ns	
RAS Precharge Time	tRP	40	-	50	-	ns	
RAS Pulse Width	tRAS	60	10,000	70	10,000	ns	
RAS Hold Time	tRSH	10	-	12	-	ns	
CAS Pulse Width	tCAS	10	10,000	12	10,000	ns	
CAS Hold Time	tCSH	40	-	50	-	ns	
RAS to CAS Delay Time	tRCD	14	45	14	52	ns	10
CAS to RAS Precharge Time	tCRP	5	-	5	_	ns	13
CAS Precharge Time	tCPN	10	-	10	-	ns	
RAS Precharge CAS Hold Time	tRPC	5	_	5	_	ns	
RAS Hold Time from CAS Precharge	tRHCP	40	-	45	_	ns	
Row Address Setup Time	tASR	5	-	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	ns	
Column Address Setup Time	tASC	0	-	0	-	ns	
Column Address Hold Time	tCAH	10	-	12	-	ns	
Column Address Lead Time Referenced to RAS	tRAL	30	-	35	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to RAS	tRRH	0	_	0	_	ns	14
Read Command Hold Time Referenced to CAS	tRCH	0	-	0	-	ns	14
WE Hold Time Referenced to CAS	tWCH	10	-	10	-		15
WE Pulse Width	tWP	10		10	_	ns	15
Data-in Setup Time	tDS	0		0	-	ns	16
Data-in Hold Time	tDH	10		10	-	ns	16
Write command Setup Time	tWCS	0	-	0	-	ns	17
CAS to WE Delay Time	tCWD	32	-	37	-	ns	17
RAS to WE Delay Time	tRWD	87		99	-	ns	17
Column Address to WE Delay Time	tAWD	52		59	-	ns	17

(2/2)

PARAMETER	SYMBOL	trac	= 60ns	trac	= 70ns	LINIET	NOTES
PARAMETER	SIMBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
WE Lead Time Referenced to RAS	tRWL	15	-	17	-	ns	
WE Lead Time Referenced to CAS	tCWL	10	-	12	-	ns	
CAS Setup Time for CAS before RAS Refresh	tCSR	5	-	5	-	ns	
CAS Hold Time for CAS before RAS Refresh	tCHR	10	-	10	-	ns	
WE Setup Time	tWSR	10	-	10	-	ns	
WE Hold Time	tWHR	15	1	15	-	ns	
Refresh Time	tREF	-	64	-	64	ms	

HYPER PAGE MODE

DADAMETER	CVO MOV	trac = 60ns		trac	= 70ns		Nome
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
Read / Write Cycle Time	tHPC	25	-	30	-	ns	
RAS Pulse Width	tRASP	60	125,000	70	125,000	ns	
CAS Pulse Width	tHCAS	10	10,000	12	10,000	ns	
CAS Precharge Time	tCP	10	-	10	-	ns	
CAS Precharge to WE Delay Time	tCPWD	52	•	59		ns	17
Read Modify Write Cycle Time	tHPRWC	66	-	75	-	ns	
Data Output Hold Time	tDHC	5	-	5	-	ns	
OE to CAS Hold Time	tOCH	5	-	5	-	ns	18
OE Precharge Time	tOEP	5	-	5	-	ns	
CAS Hold Time to OE	tCHO	5	-	5	•	ns	18
Output Buffer Turn-off Delay from WE	tWEZ	0	13	0	15	ns	12, 18
WE Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from RAS	tOFR	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from CAS	tOFC	0	13	0	15	ns	12, 18

- Notes:
 1. All voltages are referenced to GND.
 - 2. After power up, wait more than 100 µs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
 - 3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
 - 4. Specified values are obtained with outputs unloaded.
 - 5. ICC3 is measured assuming that all column address inputs are held at either high or low.
 - 6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
 - 7. ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≦VIL(MAX.) and CAS≧VIH(MIN.).
 - 8. AC measurements assume tT =2ns.

Notes:

- 9 AC Characteristics test condition
 - (1) Input timing specification

(2) Output timing specification

10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
tRAD ≤ tRAD(MAX.) and tRCD ≤ tRCD(MAX.)	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≤ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
1RCD > 1RCD(MAX.)	tCAC(MAX.)	tRCD + tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≥tRAD(MAX.) and tRCD≥tRCD(MAX.) will not cause any operation problems.

- 11. Loading conditions are 2 TTLs and 100 pF.
- 12. tOFC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
- 13. tCRP(MIN.) requirement is applied to RAS / CAS cycles preceded by any cycles.
- 14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
- 15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
- 16. tDS(MIN.) and tDH(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the WE falling edge.
- 17. If tWCS≧tWCS (MIN.), the cycle is an early write cycle and the data out will remain Hi Z through the entire cycle. If tRWD≧tRWD (MIN.), tCWD≧tCWD(MIN.), tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell.

 If neither of the above conditions is met, the state of the data out is indeterminate.
- 18. To make I/O to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) RAS, CAS: inactive (at the end of read cycle)

WE: inactive, OE: active

tOFC is effective when RAS is inactivated before CAS is inactivated.

tOFR is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)

WE: active, OE: active...tWEZ, tWPZ are effective.

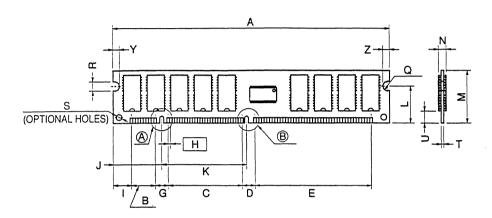
WE: inactive, OE: inactive...tOEZ is effective.

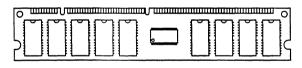
Timing Chart

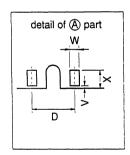
Please refer to Timing Chart 10, page 473.

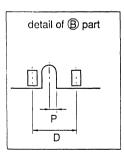
Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE) OUTLINE DRAWINGS









ITEM	MILLIMETERS	INCHES
Ä	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
1	8.89	0.350
J	23.495	0.925
К	42.18	1.661
L	17.78	0.700
М	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Р	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157+0.005
S	φ3.0	φ0.118
т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
×	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.
		M168S-50A2



MC-424000LFC72F

3.3 V OPERATION 4M -WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (ECC)

Description

The MC-424000LFC72F is a 4 194 304 words by 72 bits dynamic RAM module on which 18 pieces of 16M DRAM (μ PD 4216405L) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4 194 304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)		
	(1117 01.7	(IVIIIV.)	Cycle anne (mire.)	Active	Standby	
MC- 424000LFC72-A60	60 ns	104 ns	25 ns	5.87 w	180 mw	
MC- 424000LFC72-A70	70 ns	124 ns	30 ns	5.22 w	(CMOS level)	

- 4 096 refresh cycles/64 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3 V±0.3V power supply

Ordering information

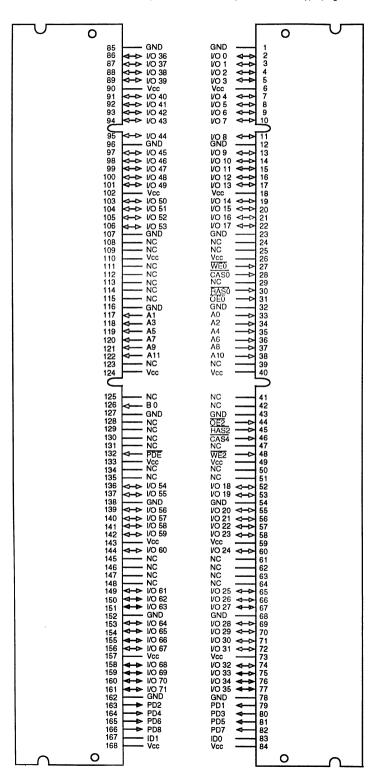
Part Number	Access time (MAX.)	Package	Mounted devices
MC- 424000LFC72F-A60	60ns	168-pin Dual In-line Memory Module	18 pieces of uPD 4216405LG3
MC- 424000LFC72F-A70	70ns	(Socket Type) Edge connector: Gold plating	(300mil TSOP) [Double side]

The information in this document is subject to change without notice.

110043EJ4V0DS00 (Japan) 355

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



PD and ID Table

Pin	Pin	Accse	ss Time
Name	No.	60ns	70ns
PD1	79	Н	Н
PD2	163	Ι	Н
PD3	80	٦	L
PD4	164	H	Н
PD5	81	Н	Н
PD6	165	Ι	L
PD7	82	Ι	Н
PD8	166	٦	L
I D0	83	GND	GND
I D1	167	GND	GND

Note) H: VOH, L: VOL

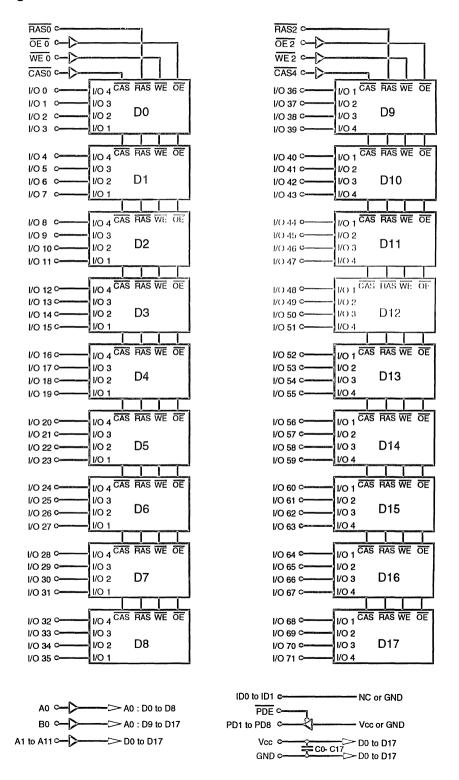
A0 - A11, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
FAS0, RAS2 : Row Address Strobe
CAS0, CAS4 : Column Address Strobe
WED WE9 : Write Enable

WE0, WE2 : Write Enable
OE0, OE2 : Output Enable

PDE : Presence Detect Enable
PD1- PD8 : Presence Detect Pins
ID0, ID1 : Identity pins
Vcc : Power Supply

GND : Ground NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +4.6	V
Supply voltage	VCC		-0.5 to +4.6	V
Output current	IO		20	mA
Power dissipation	PD		20	W
Operating temperature	Topt		0 to +70	${\mathfrak C}$
Storage temperature	Tstg		-55 to +125	${\mathfrak C}$

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES:1,2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	v
High level input voltage	VIH		2.0		Vcc + 0.3	v
Low level input voltage	VIL		-0.3		+0.8	v
Ambient temperature	Ta		0		70	v

CAPACITANCE (Ta=25 $^{\circ}$ C, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
	CI1	A0 - A11, B0			20	pF
Input capacitance	CI2	WE 0, WE 2			20	pF
	C 1 3	RAS 0, RAS 2			78	pF
	C I 4	CAS 0, CAS 4			20	pF
	C I 5	OE 0, OE 2			20	pF
Data Input/ Output capacitance	C 1/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
		RAS, CAS Cycling	trac=60ns		1 450	mA	2.4.7
Operating Current	Icc1	trc=trc (MIN.), IO=0mA	trac=70ns		1 270	IIIA	3, 4, 7
Standby Current	Icc2	RAS, CAS ≥ VIH(MIN.)			100	mA	
Standoy Carroni	1002	$\overline{\text{RAS}}$, $\overline{\text{CAS}} \ge \text{Vcc-0.2V}$			50	ша	
DAC only refeesh surrent	Icc3	RAS Cycling, CAS ≥ V _{IH}	trac=60ns		1 450	A	2 4 5 5
RAS only refresh current	1003	trc=trc(min.), IO=0mA	trac=70ns		1 270	mA	3, 4, 5, 7
Operating Current	Icc4	RAS ≤ VIL, CAS Cycling	trac=60ns		1 630	A	2.4.6
(Hyper Page Mode)		tHPC=tHPC (MIN.), IO=0mA	trac=70ns		1 450	mA	3, 4, 6
CAS before RAS	Icc5	trc=trc (MIN.)	trac=60ns	1 450	mA	2.4	
refresh current	1005	IO=0mA	trac=70ns		1 270	ша	3, 4
Input Leakage Current	Υ	VI=0 to 3.6V	RAS	-5	+5		
Input Leakage Current	Iı(L)	all other pins not under test = 0V	others	-5	+1	μΑ	
Output Leslings Cument	-	Outputs are disabled (Hi - Z)		_	_		
Output Leakage Current	Io(L)	VO=0 to 3.6V		-5	+5	μА	
High level output voltage	Vон	IO=-2.0mA		2.4		V	
Low level output voltage	Vol	IO=+2.0mA			0.4	v	

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

DAD ANGEDER		trac:	= 60ns	trac	trac = 70ns		NOTES
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.		NOTES
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157		ns	
Access Time from RAS	tRAC		60		70	ns	10,11
Access Time from CAS	tCAC		20		23	ns	10,11
Access Time from Column Address	tAA	_	35	-	40	ns	10,11
Access Time from CAS Precharge	tACP		40		45	ns	11
Access Time from OE	tOEA	-	20	-	23	ns	11
RAS to Column Address Delay Time	tRAD	12	30	12	35	ns	10
CAS to Data Setup Time	tCLZ	0	-	0	-	ns	11
OE to Data Setup Time	tOLZ	0	-	0	-	ns	11
OE to Data Delay Time	tOED	13		15	-	ns	
Output Buffer Turn-off Delay Time from OE	tOEZ	0	13	0	15	ns	12
OE Hold Time	tOEH	0	-	0	-	ns	
OE Lead Time Referenced to RAS	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
RAS Precharge Time	tRP	40	-	50	-	ns	
RAS Pulse Width	tRAS	60	10,000	70	10,000	ns	
RAS Hold Time	tRSH	10	-	12	-	ns	
CAS Pulse Width	tCAS	10	10,000	12	10,000	ns	
CAS Hold Time	tCSH	40	-	50	-	ns	
RAS to CAS Delay Time	tRCD	14	45	14	52	ns	10
CAS to RAS Precharge Time	tCRP	5	-	5	-	ns	13
CAS Precharge Time	tCPN	10	-	10	-	ns	
RAS Precharge CAS Hold Time	tRPC	5	•	5	-	ns	
RAS Hold Time from CAS Precharge	tRHCP	40	-	45	-	ns	
Row Address Setup Time	tASR	5	_	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	ns	
Column Address Setup Time	tASC	0	-	0	-	ns	
Column Address Hold Time	tCAH	10	_	12	-	ns	
Column Address Lead Time Referenced to RAS	tRAL	30	-	35	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to RAS	tRRH	0	-	0	-	ns	14
Read Command Hold Time Referenced to CAS	tRCH	0	-	0	-	ns	14
WE Hold Time Referenced to CAS	tWCH	10	_	10	-		15
WE Pulse Width	tWP	10	-	10	-	ns	15
Data-in Setup Time	tDS	0		0		ns	16
Data-in Hold Time	tDH	10		10	_	ns	16
Write command Setup Time	tWCS	0	_	0	-	ns	17
CAS to WE Delay Time	tCWD	32	_	37	-	ns	17
RAS to WE Delay Time	tRWD	87	_	99	-	ns	17
Column Address to WE Delay Time	tAWD	52	_	59	_	ns	17

(2/2)

DADAMETED	SYMBOL	trac =		trac	= 70ns	UNIT	NOTES
PARAMETER	SI MIBOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
WE Lead Time Referenced to RAS	tRWL	15	-	17	-	ns	
WE Lead Time Referenced to CAS	tCWL	10	-	12		ns	
CAS Setup Time for CAS before RAS Refresh	tCSR	5	-	5		ns	
CAS Hold Time for CAS before RAS Refresh	tCHR	10	-	10	-	ns	
WE Setup Time	tWSR	10	-	10	•	ns	
WE Hold Time	tWHR	15	-	15		ns	
Refresh Time	tREF	-	64	-	64	ms	

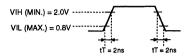
HYPER PAGE MODE

DADAMETER	SYMBOL	trac = 60ns		trac = 70ns		LINIE	Nomen
PARAMETER	STWIDOL	MIN.	MAX.	MIN.	MAX.	UNII	NOTES
Read / Write Cycle Time	tHPC	25	-	30	,	ns	
RAS Pulse Width	tRASP	60	125,000	70	125,000	ns	
CAS Pulse Width	tHCAS	10	10,000	12	10,000	ns	
CAS Precharge Time	tCP	10	-	10	-	ns	
CAS Precharge to WE Delay Time	tCPWD	52	-	59		ns	17
Read Modify Write Cycle Time	tHPRWC	66	-	75	-	ns	
Data Output Hold Time	tDHC	5	-	5	-	ns	
OE to CAS Hold Time	tOCH	5	-	5	-	ns	18
OE Precharge Time	tOEP	5		5	-	ns	
CAS Hold Time to OE	tCHO	5	-	5	-	ns	18
Output Buffer Turn-off Delay from WE	tWEZ	0	13	0	15	ns	12, 18
WE Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from RAS	tOFR	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from CAS	tOFC	0	13	0	15	ns	12, 18

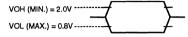
- Notes:
 1. All voltages are referenced to GND.
 - 2. After power up, wait more than 100 µs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
 - 3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
 - 4. Specified values are obtained with outputs unloaded.
 - 5. ICC3 is measured assuming that all column address inputs are held at either high or low.
 - 6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
 - 7. ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≦VIL(MAX.) and CAS≧VIH(MIN.).
 - 8. AC measurements assume tT =2ns.

Notes:

- 9. AC Characteristics test condition
 - (1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$tRAD \le tRAD(MAX.)$ and $tRCD \le tRCD(MAX.)$	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≤ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
tRCD > tRCD(MAX.)	tCAC(MAX.)	tRCD + tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≥tRAD(MAX.) and tRCD≥tRCD(MAX.) will not cause any operation problems.

- 11. Loading conditions are 1 TTLs and 100 pF.
- 12. tOFC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
- 13. tCRP(MIN.) requirement is applied to RAS / CAS cycles preceded by any cycles.
- 14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
- 15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
- 16. tDS(MIN.) and tDH(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the WE falling edge.
- 17. If tWCS≧tWCS (MIN.), the cycle is an early write cycle and the data out will remain Hi Z through the entire cycle. If tRWD≧tRWD (MIN.), tCWD≧tCWD(MIN.), tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell.

 If neither of the above conditions is met, the state of the data out is indeterminate.
- 18. To make I/O to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) RAS, CAS: inactive (at the end of read cycle)

WE: inactive, OE: active

tOFC is effective when RAS is inactivated before CAS is inactivated.

tOFR is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)

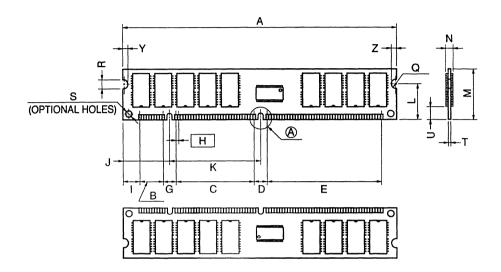
WE: active, OE: active...tWEZ, tWPZ are effective.

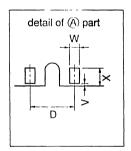
WE: inactive, OE: inactive...tOEZ is effective.

Timing Chart

Please refer to Timing Chart 10, page 473.

Package Drawing



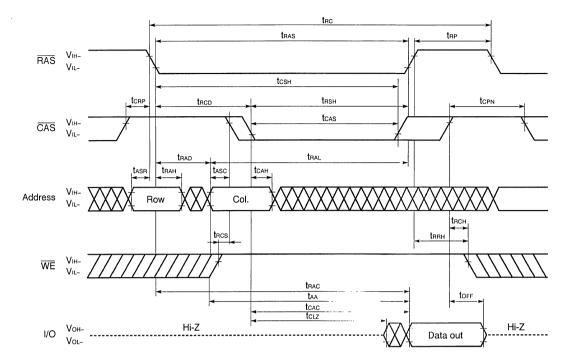


ITEM	MILLIMETERS	INCHES
Α	133.35±0.13	5.25±0.006
В	11.43	0.450
С	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
Н	1.27 (T.P.)	0.050 (T.P.)
1	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} -0.004
S	φ3.0	φ0.118
Т	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
٧	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

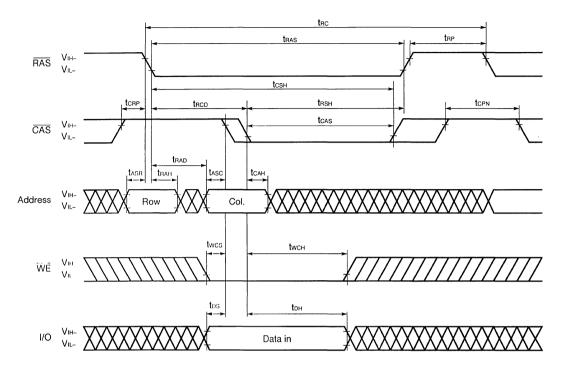
M168S-50A3

Timing Chart 1

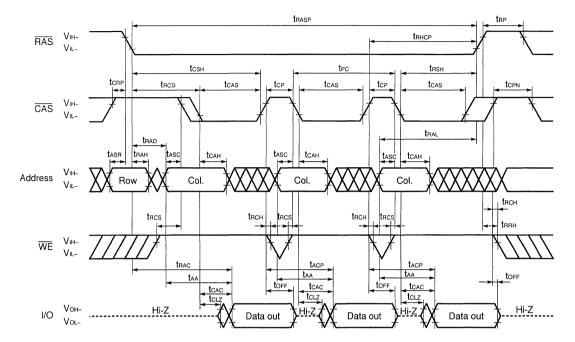
Read Cycle



Early Write Cycle

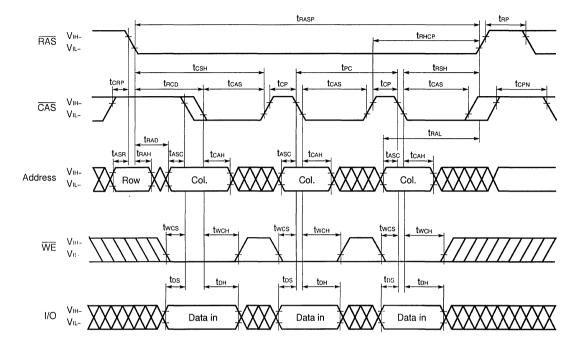


Fast Page Mode Read Cycle



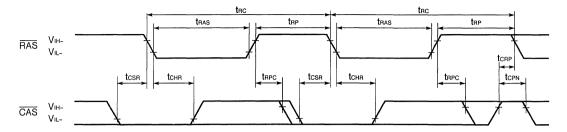
Remark In the fast page mode, read and write cycles are available for each of the consecutive \overline{CAS} cycles within the same \overline{RAS} cycle.

Fast Page Mode Early Write Cycle



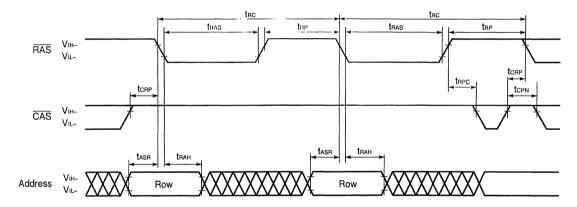
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



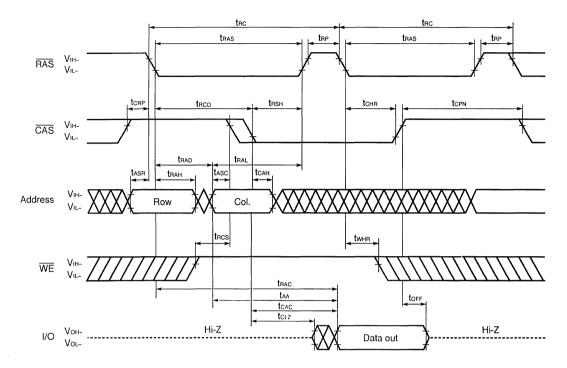
Remark Address, WE: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

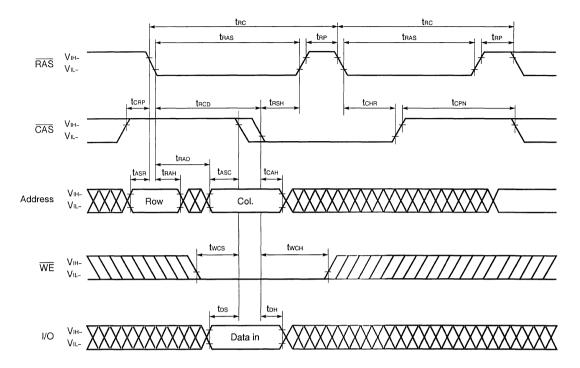


Remark WE: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



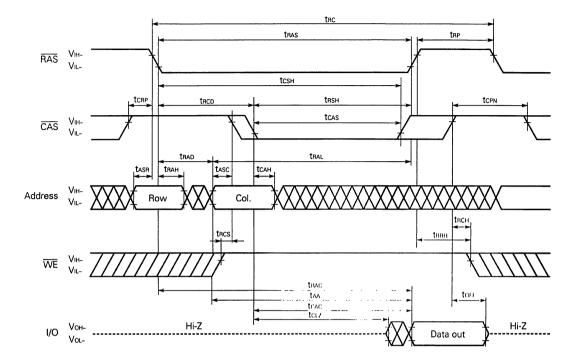
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	•		

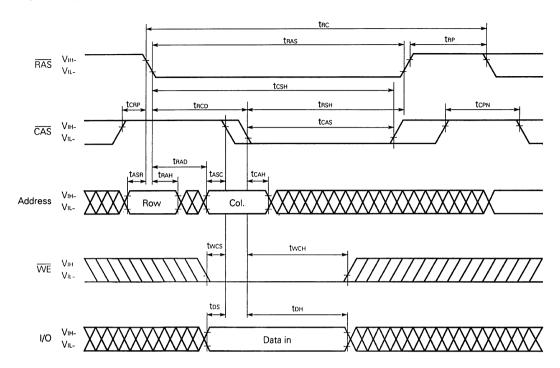
Timing Chart 2

		,

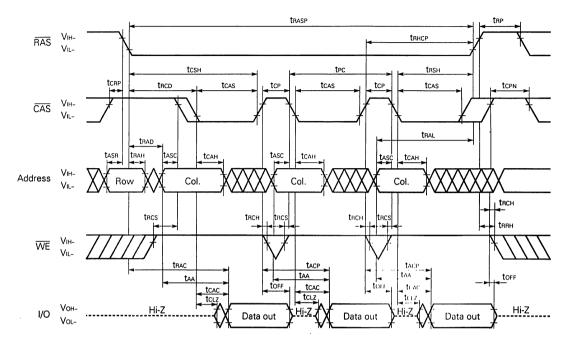
Read Cycle



Early Write Cycle

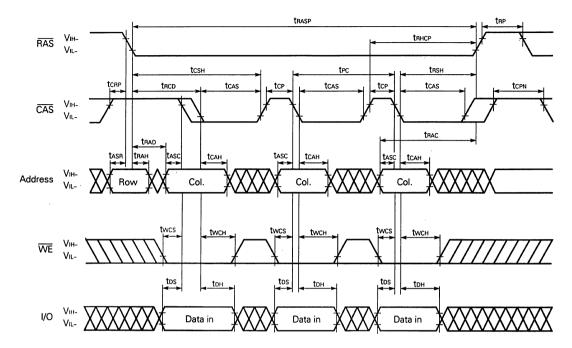


Fast Page Mode Read Cycle



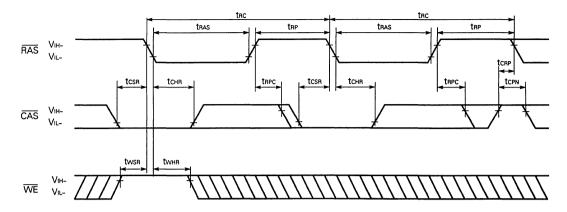
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



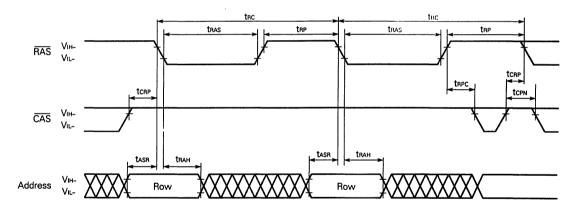
Remark In the fast page mode, read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



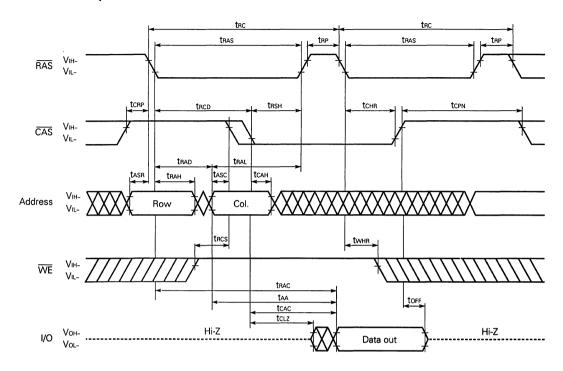
Remark Address: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

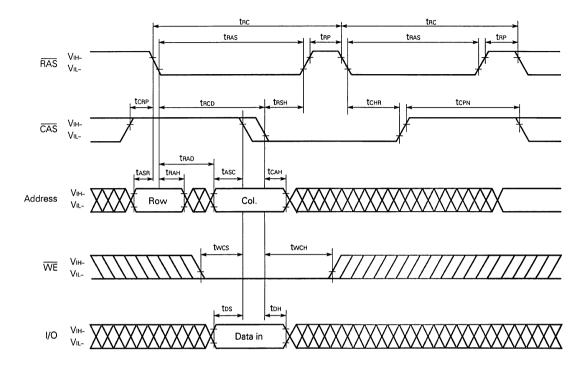


Remark WE: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

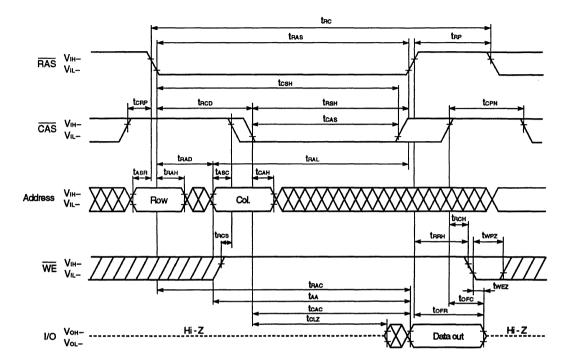


Hidden Refresh Cycle (Write)

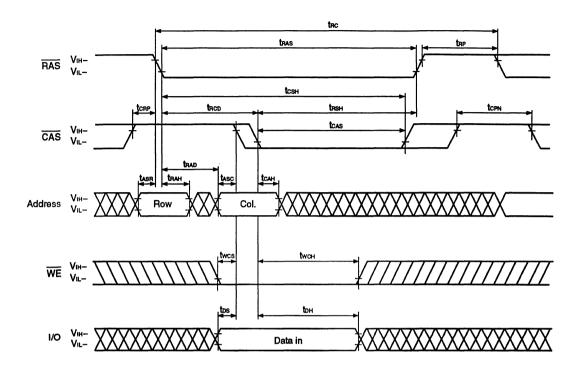


Timing Chart 3

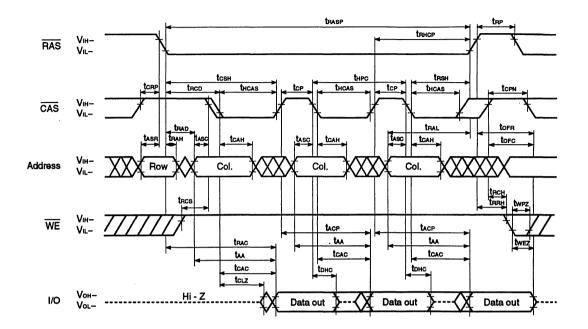
Read Cycle



Early Write Cycle

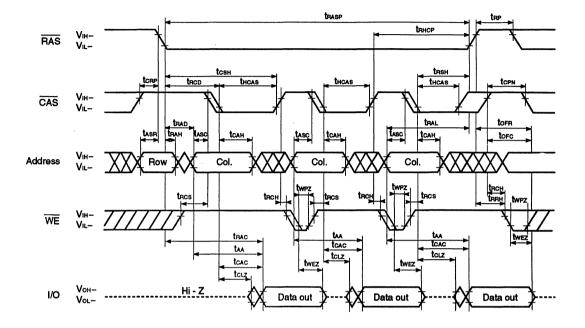


Hyper Page Mode Read Cycle



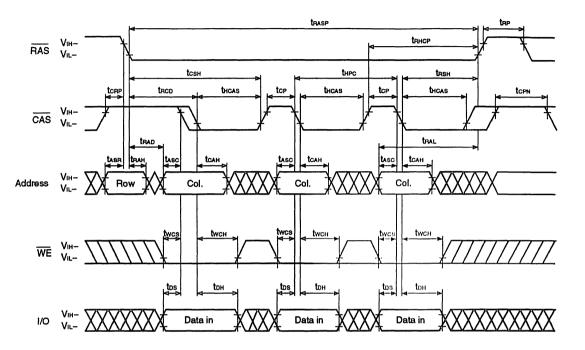
Remark In the hyper page mode,read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Cycle (WE Control)



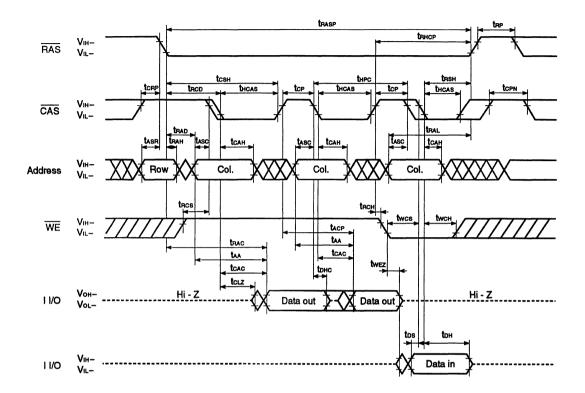
Remark In the hyper page mode, read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Early Write Cycle



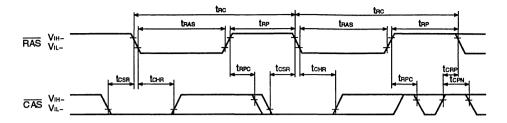
Remark In the hyper page mode,read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read and Write Cycle



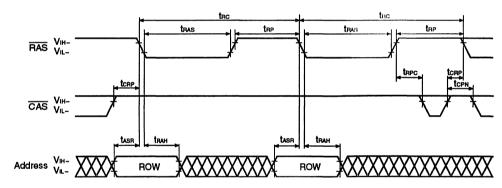
Remark In the hyper page mode,read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



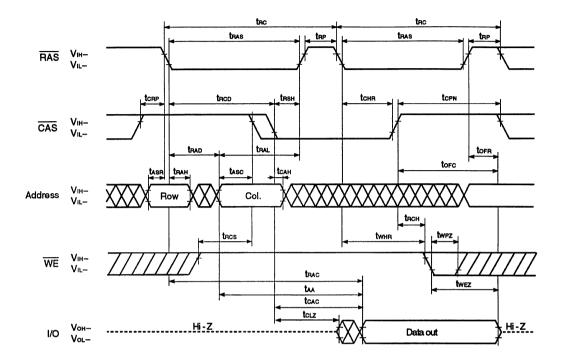
Remark Address,WE = Don't care VO = Hi - Z

RAS Only Refresh Cycle

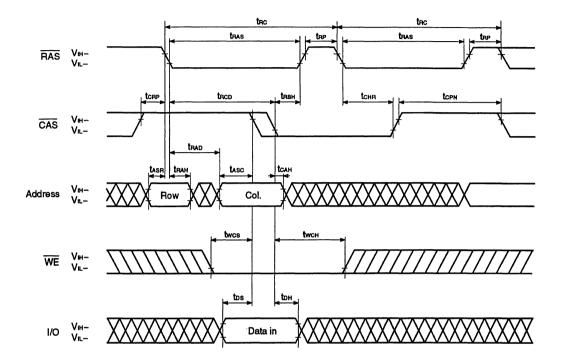


Remark WE = Don't care , I/O = Hi - Z

Hidden Refresh Cycle (Read)

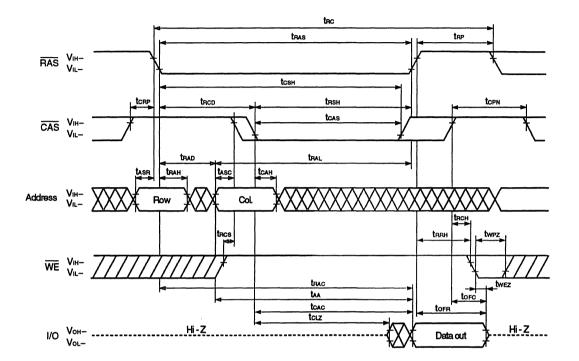


Hidden Refresh Cycle (Write)

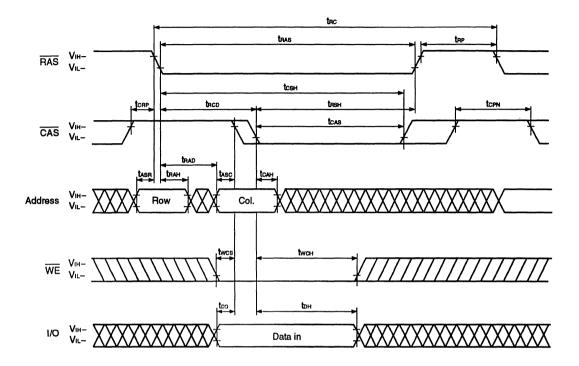


Timing Chart 4

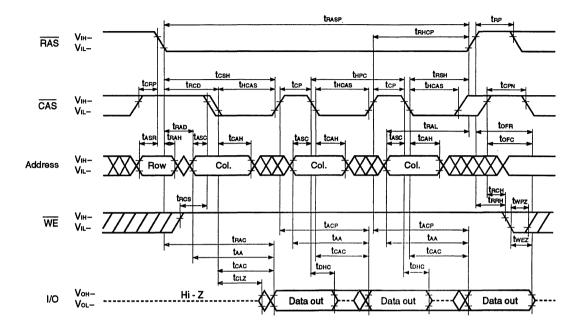
Read Cycle



Early Write Cycle

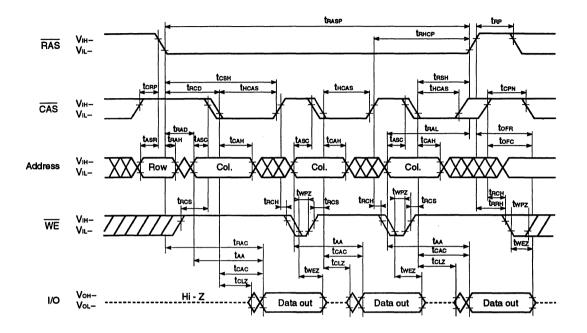


Hyper Page Mode Read Cycle



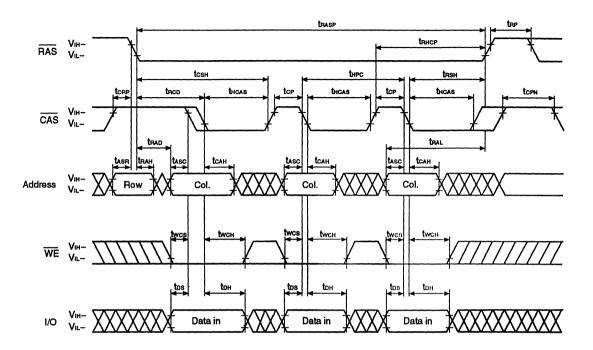
Remark In the hyper page mode,read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Cycle (WE Control)



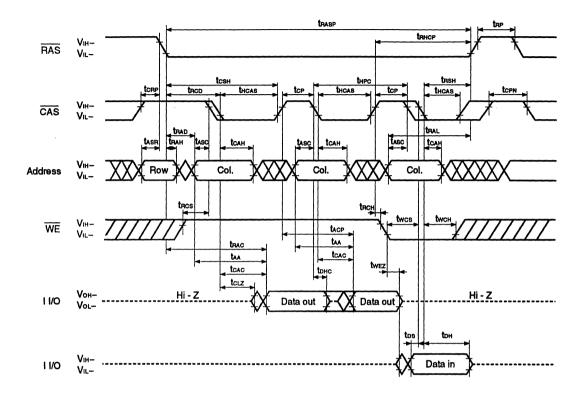
Remark In the hyper page mode,read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Early Write Cycle



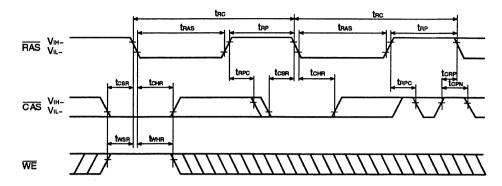
Remark In the hyper page mode,read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read and Write Cycle



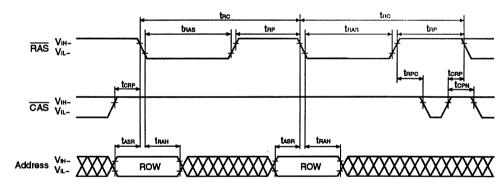
Remark In the hyper page mode,read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



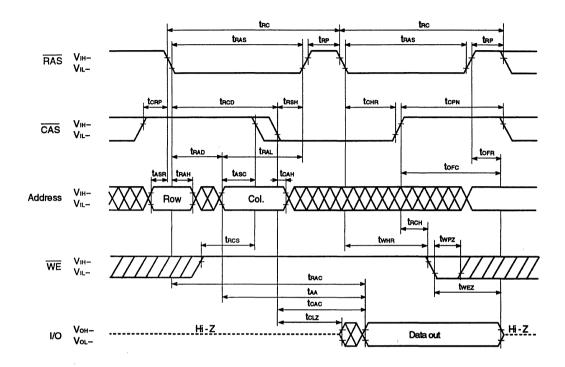
Remark Address = Don't care I/O = Hi - Z

RAS Only Refresh Cycle

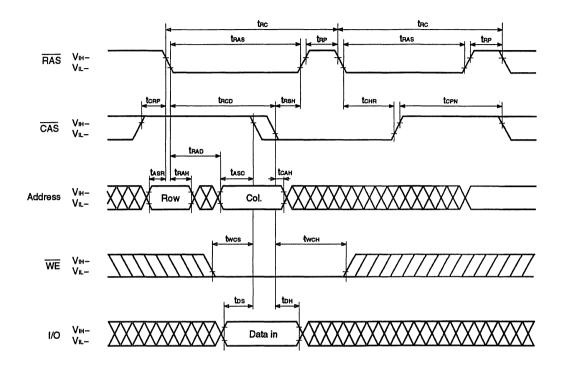


Remark WE - Don't care , I/O - Hi - Z

Hidden Refresh Cycle (Read)



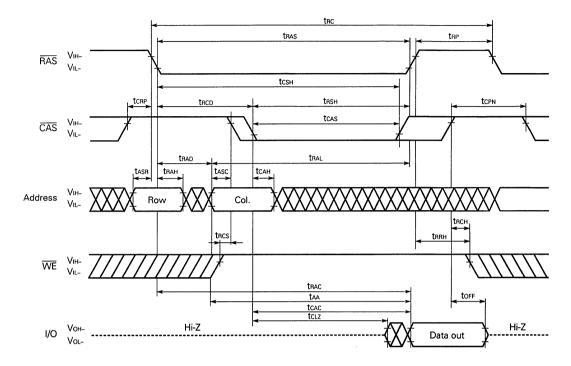
Hidden Refresh Cycle (Write)



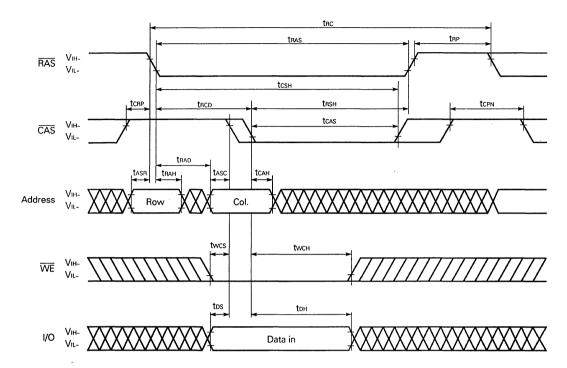


Timing Chart 5

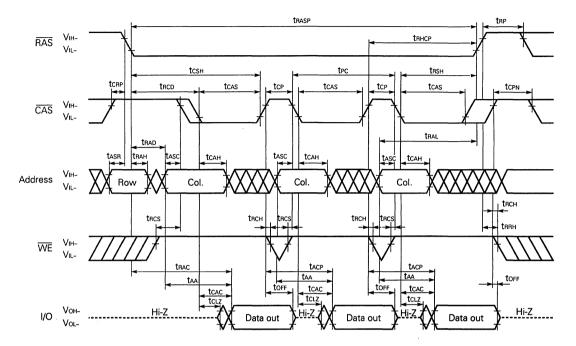
Read Cycle



Early Write Cycle

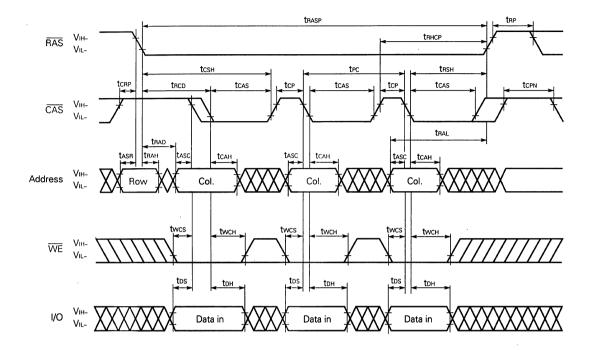


Fast Page Mode Read Cycle



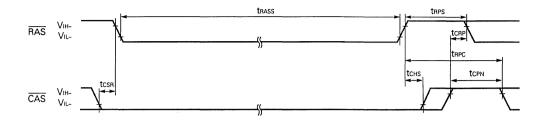
Remark In the fast page mode, read and write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle



Remark Address, WE: Don't care I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

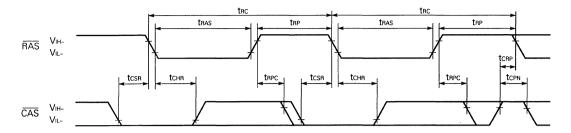
- (1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.
- (2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

 When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform

 RAS only refresh 1,024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

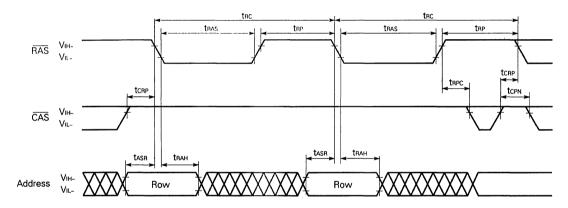
For details, please refer to How to use DRAM User's Manual.

CAS Before RAS Refresh Cycle



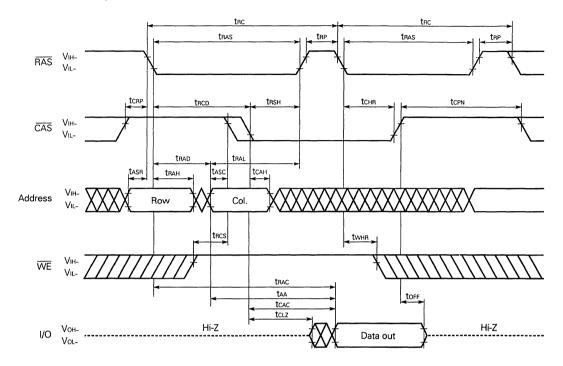
Remark Address, WE: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

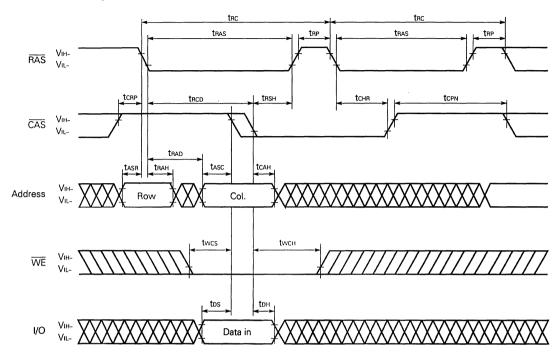


Remark WE: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

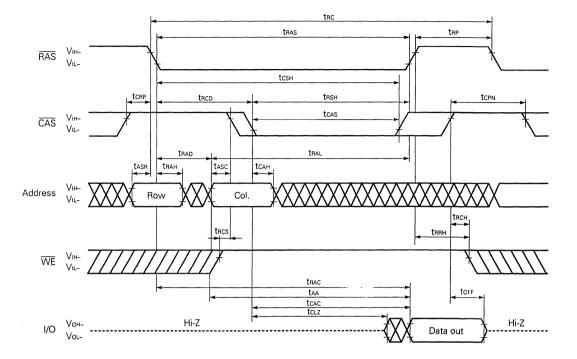


Hidden Refresh Cycle (Write)

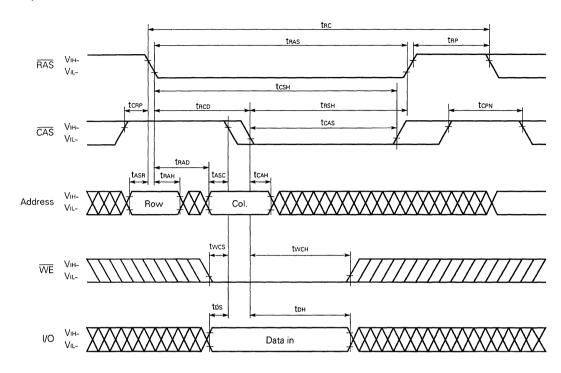


Timing Chart 6

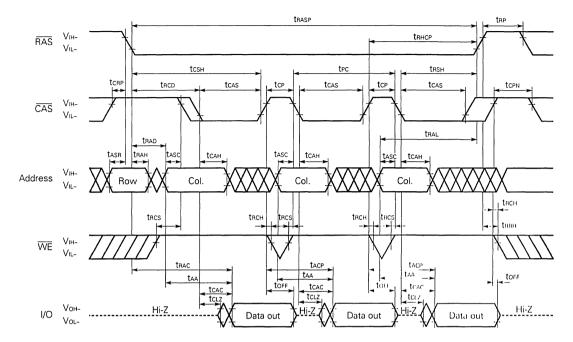
Read Cycle



Early Write Cycle

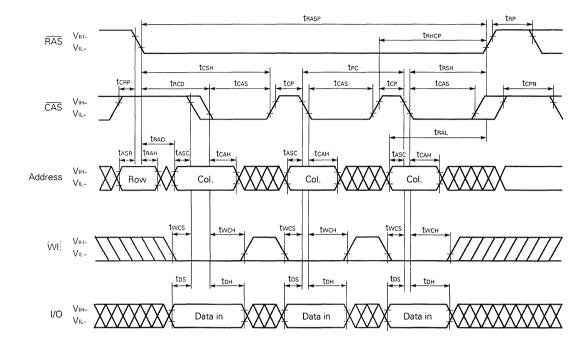


Fast Page Mode Read Cycle



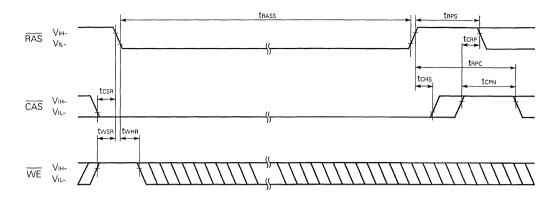
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle



Remark Address: Don't care I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

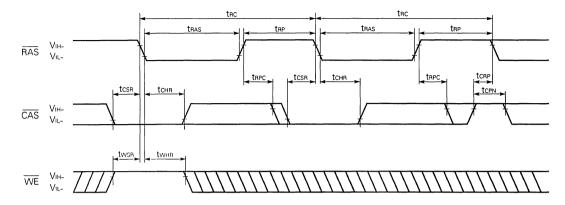
 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with long $\overline{\text{RAS}}$ only refresh (both distributed and burst), the following cautions must be observed.

- (1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh
 When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please
 perform CAS before RAS refresh 2,048 times within a 32 ms interval just before and after setting CAS
 before RAS self refresh.
- (2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

 When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

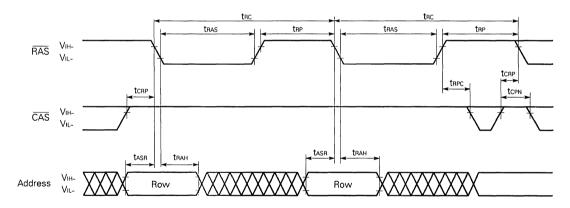
For details, please refer to How to use DRAM User's Manual.

CAS Before RAS Refresh Cycle



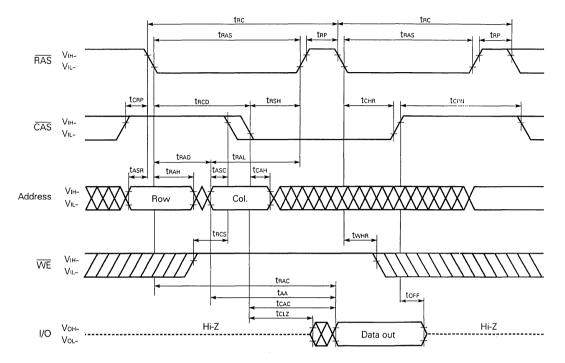
Remark Address: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

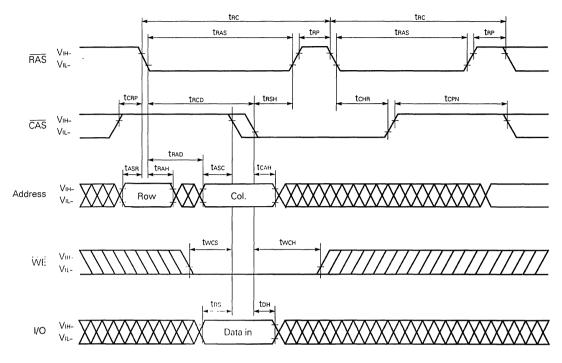


Remark WE: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



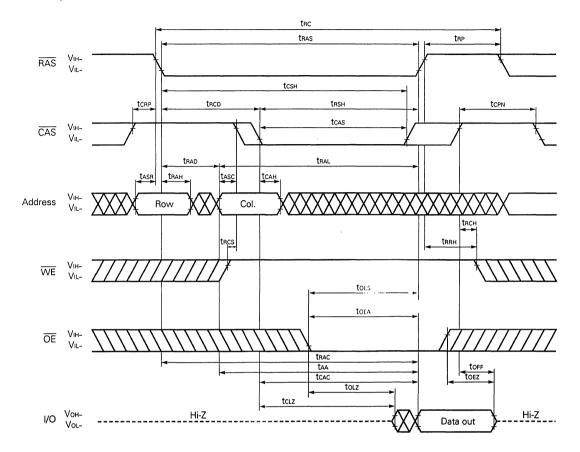
Hidden Refresh Cycle (Write)



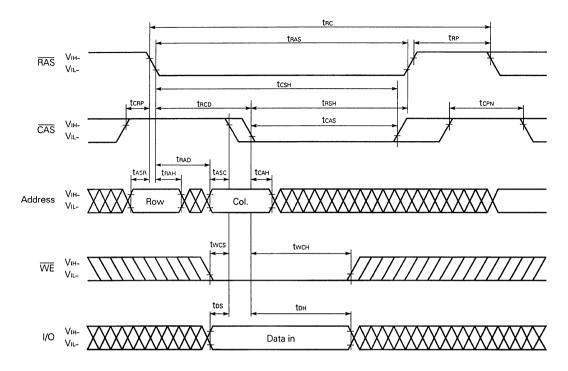
Timing Chart 7



Read Cycle

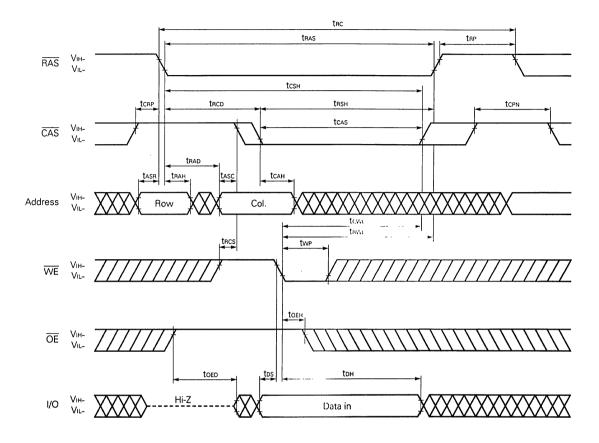


Early Write Cycle

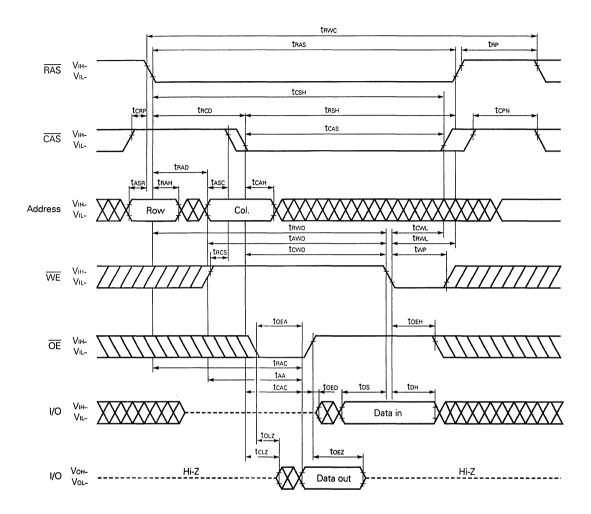


Remark OE: Don't care

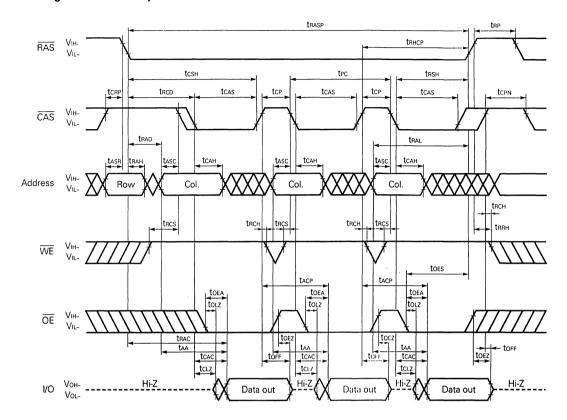
Late Write Cycle



Read Modify Write Cycle

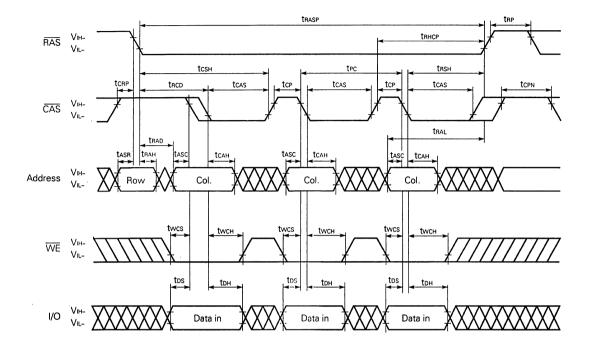


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

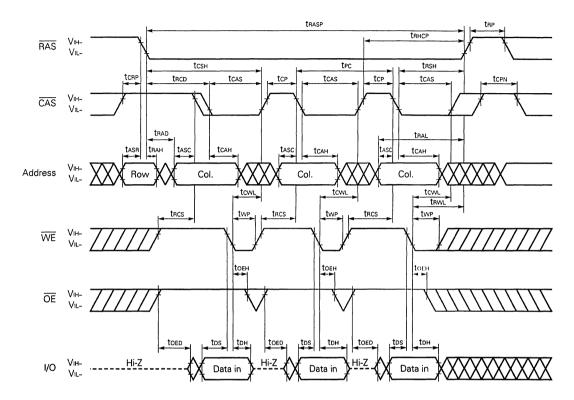
Fast Page Mode Early Write Cycle



Remark OE: Don't care

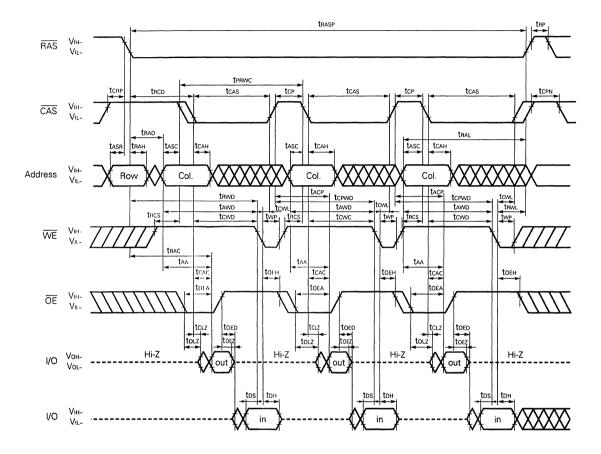
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle



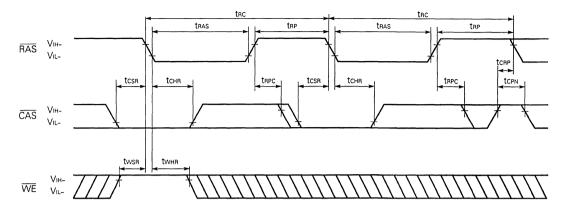
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Read Modify Write Cycle



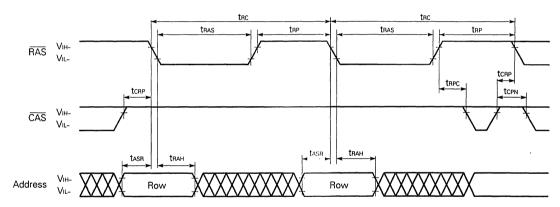
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



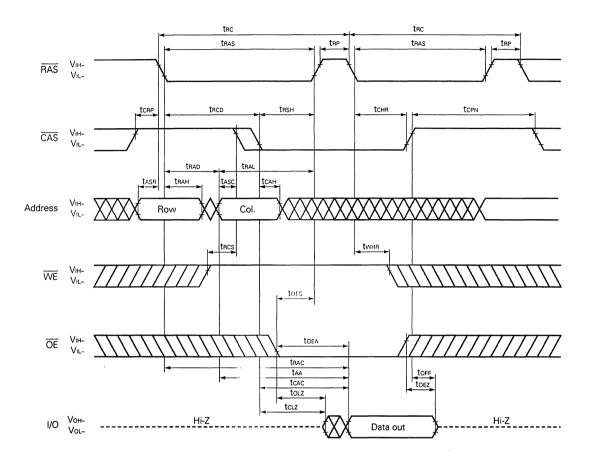
Remark Address, OE: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

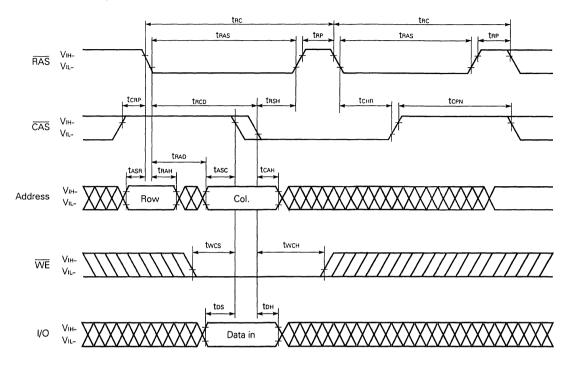


Remark WE, OE: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

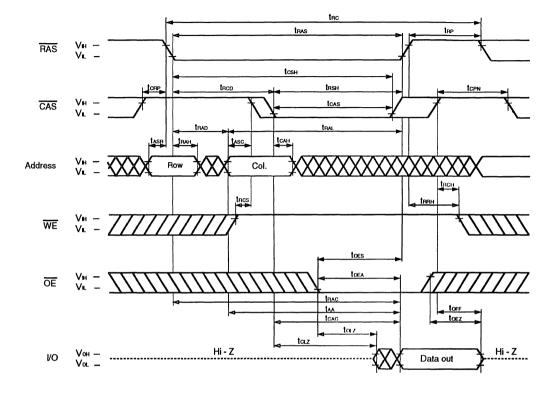


Remark OE : Don't care

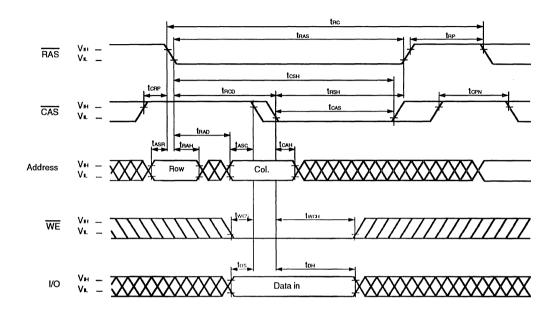


Timing Chart 8

Read Cycle

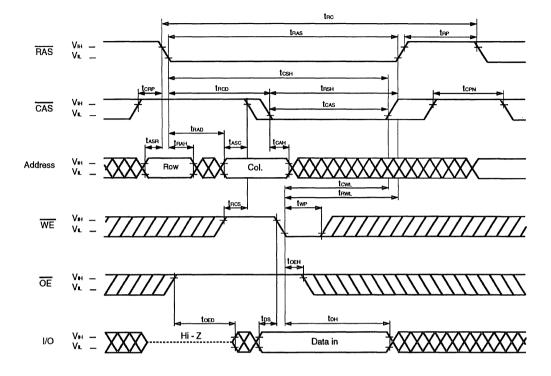


Early Write Cycle

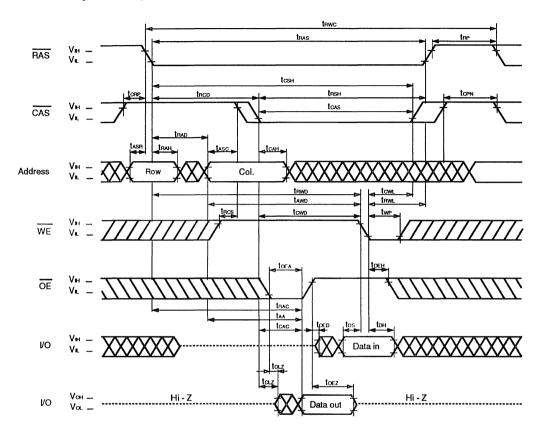


Remark OE: Don't care

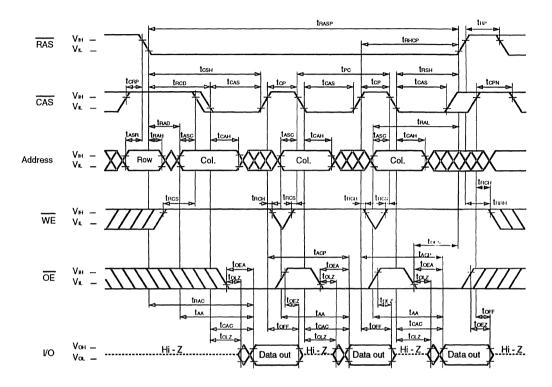
Late Write Cycle



Read Modify Write Cycle

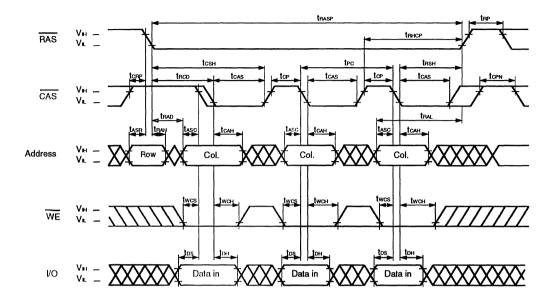


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

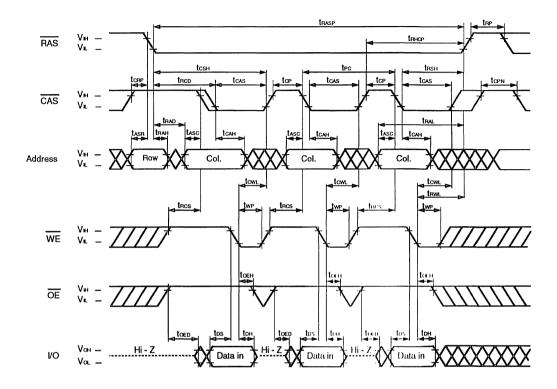
Fast Page Mode Early Write Cycle



Remark OE : Don't care

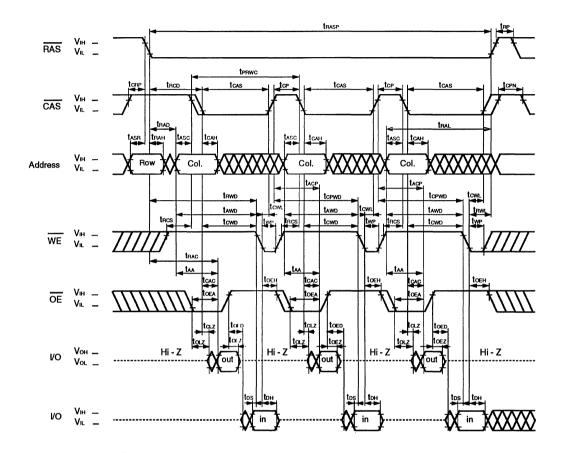
In the fast page mode, read, <u>write</u> and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Late Write Cycle



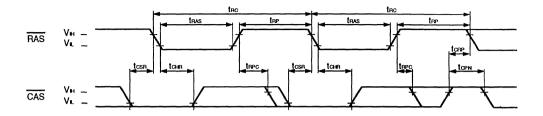
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Read Modify Write Cycle



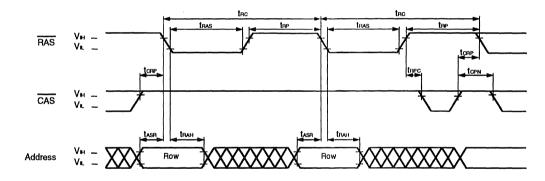
Remark In the fast page mode, read, <u>write</u> and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



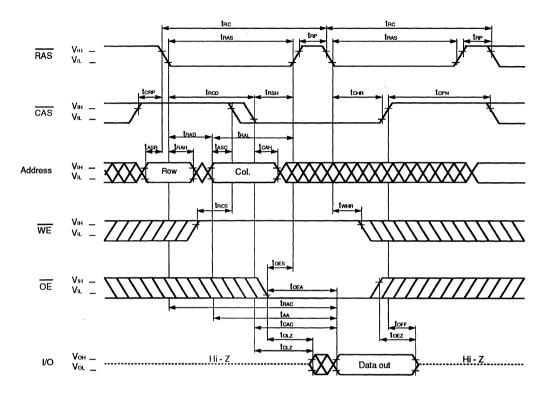
Remark Address, WE, OE: Don't care I/O: Hi - Z

RAS Only Refresh Cycle

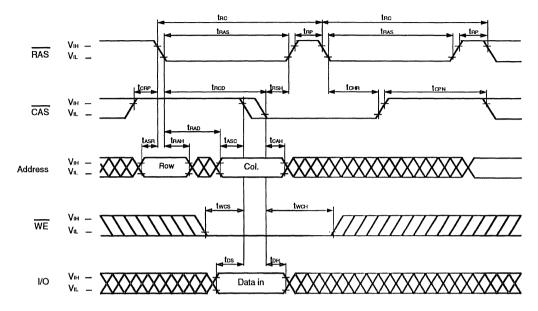


Remark WE, OE: Don't care I/O: Hi - Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

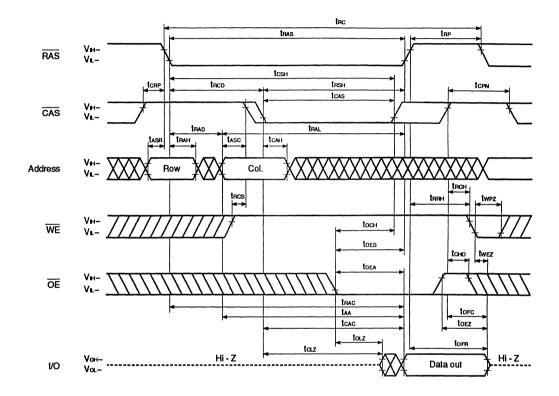


Remark OE: Don't care

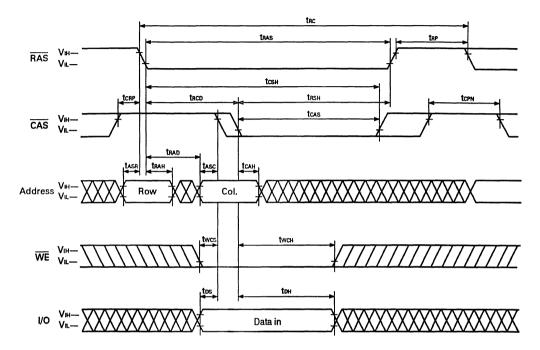
	,	

Timing Chart 9

Read Cycle

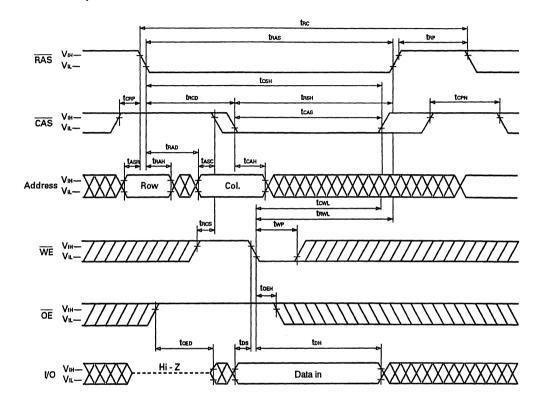


Early Write Cycle

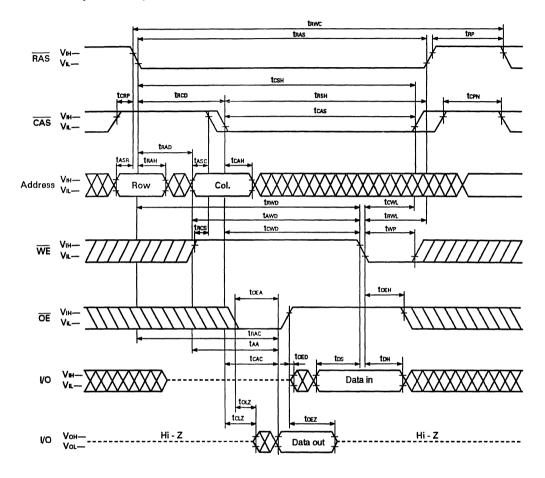


Remark OE : Don't care

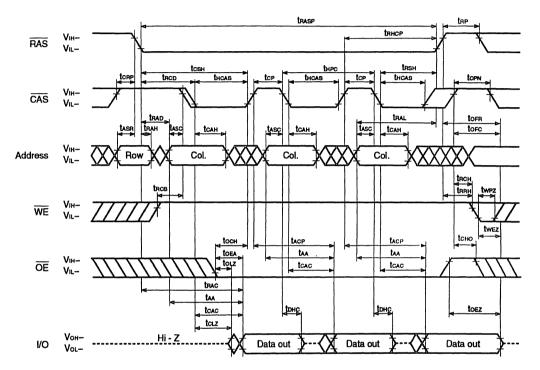
Late Write Cycle



Read Modify Write Cycle

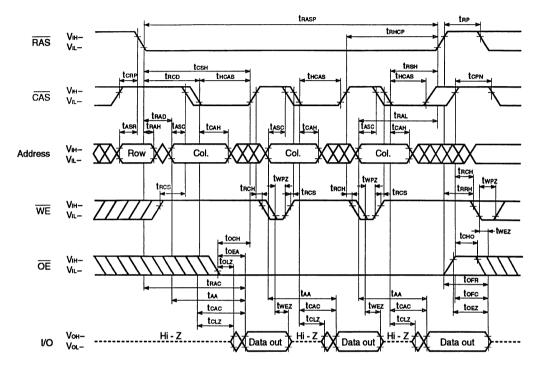


Hyper Page Wode Read Cycle



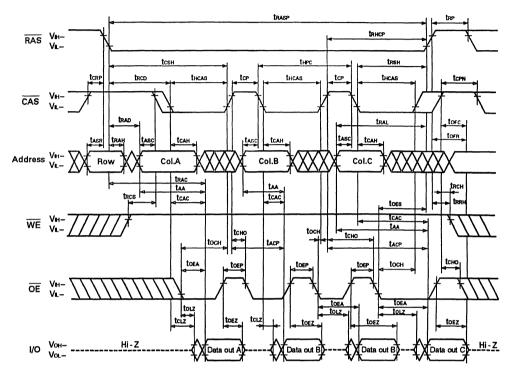
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Cycle (WE Control)



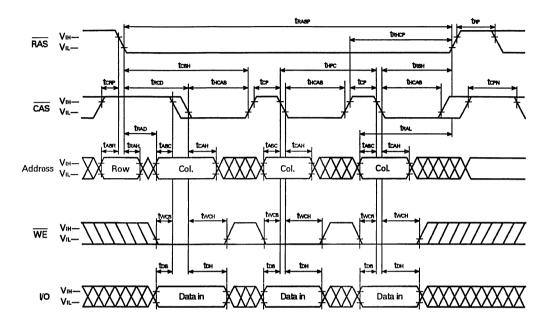
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Cycle (OE Control)



Romark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

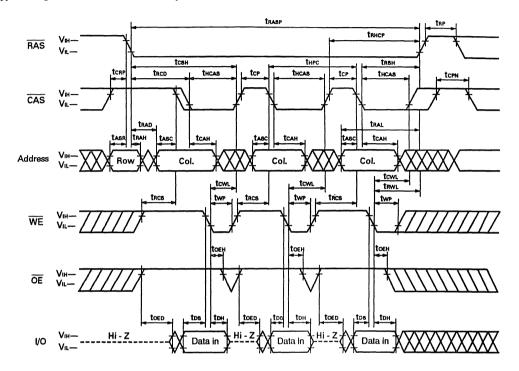
Hyper Page Mode Early Write Cycle



Remark 1. OE: Don't care

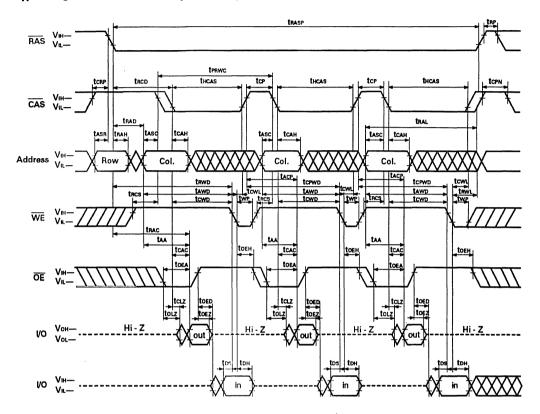
2. In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Late Write Cycle



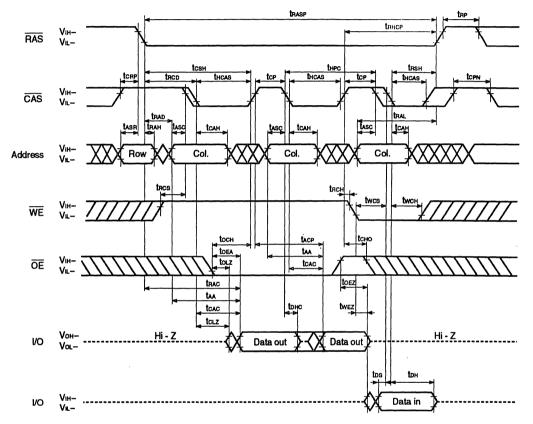
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Modify Write Cycle



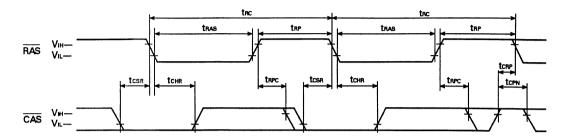
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read and Write Cycle



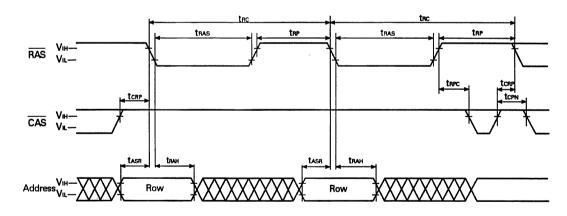
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



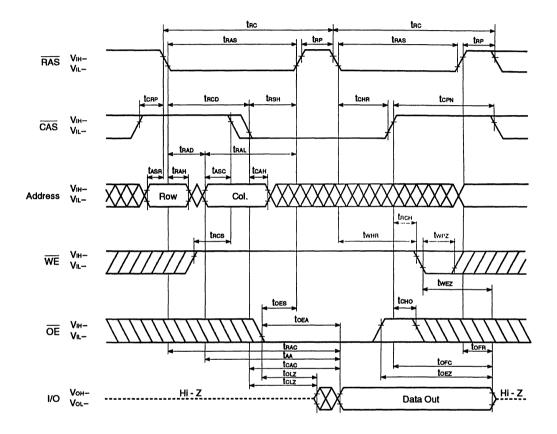
Remark Address, WE, OE: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

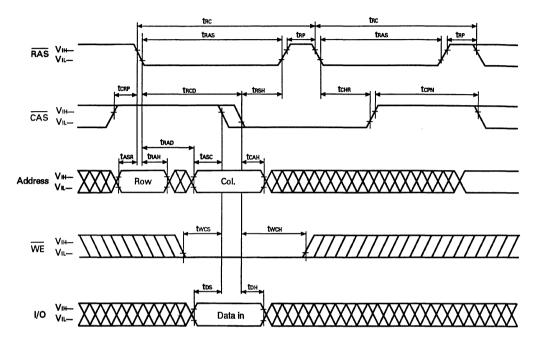


Remark WE, OE: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

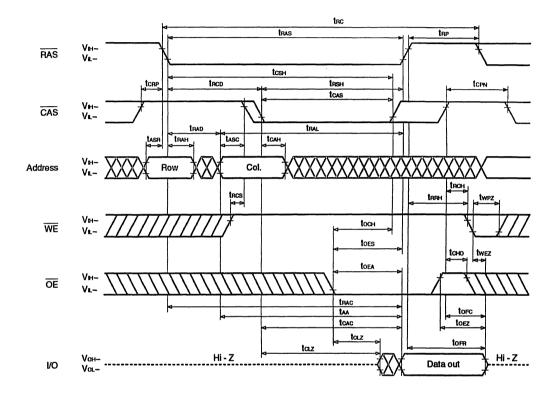


Remark OE : Don't care

Timing Chart 10

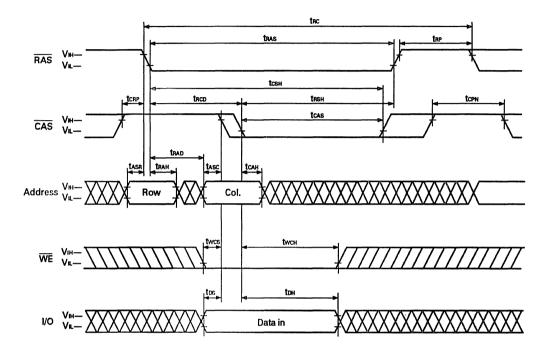


Road Cyclo



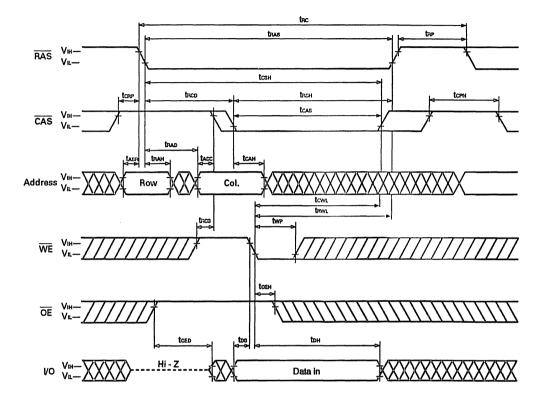
475

Early Write Cycle

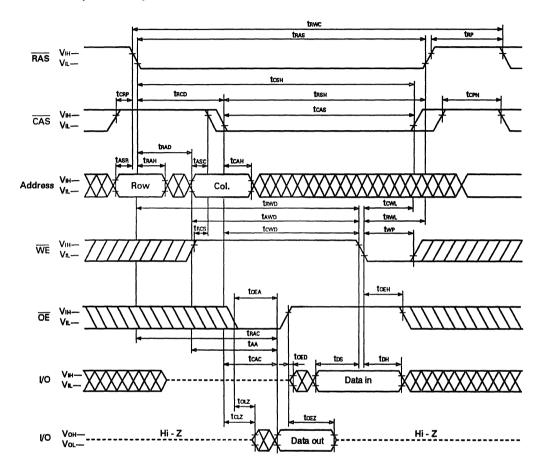


Remark OE: Don't care

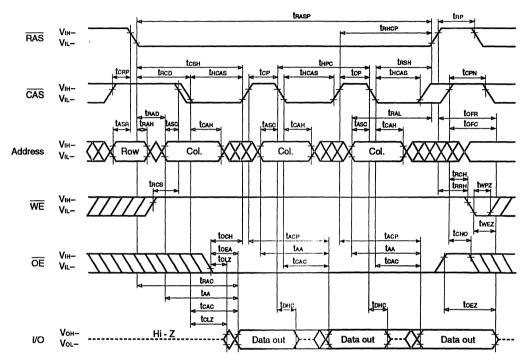
Lato Write Cycle



Read Modify Write Cycle

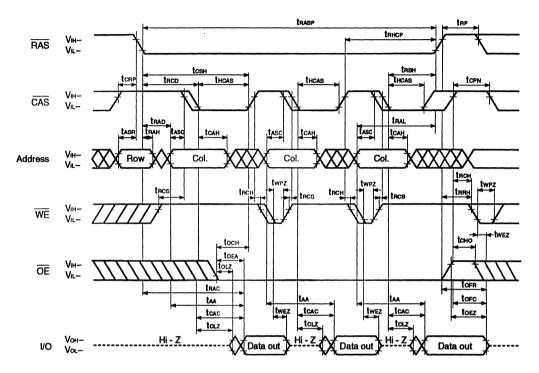


Hyper Page Mode Read Cycle



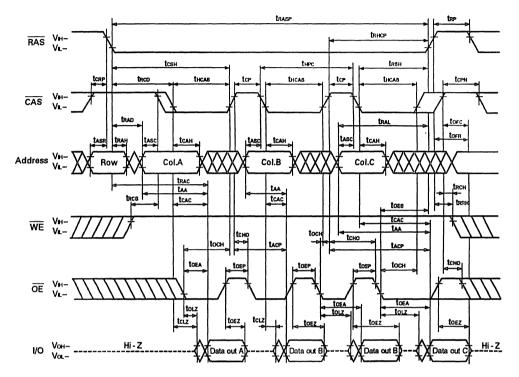
Romark In the hyper page mode, read,write and road modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Cycle (WE Control)



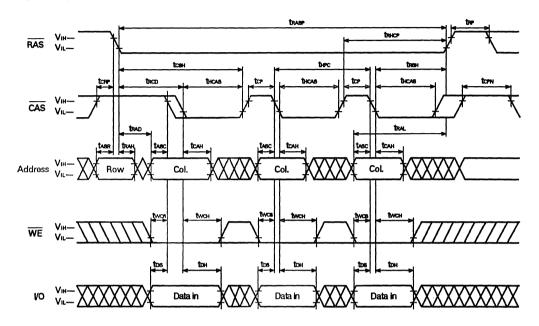
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Cycle (OE Control)



Romark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

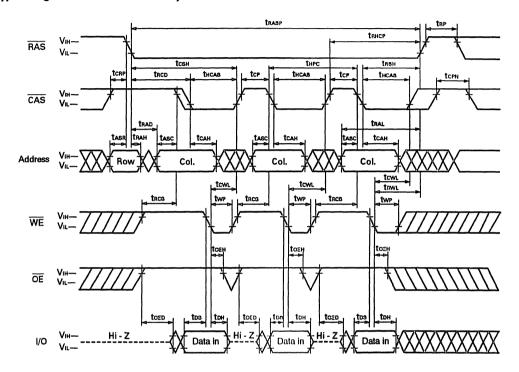
Hyper Page Mode Early Write Cycle



Remark 1. OE: Don't care

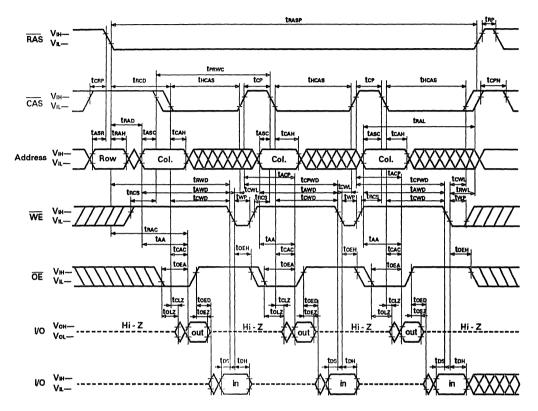
2. In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hypor Page Mode Late Write Cycle



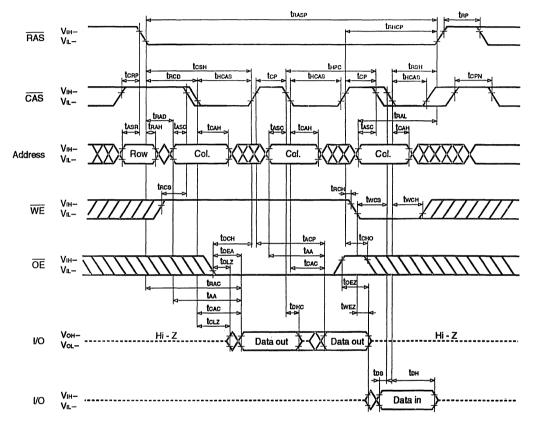
Romark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read Modify Write Cycle



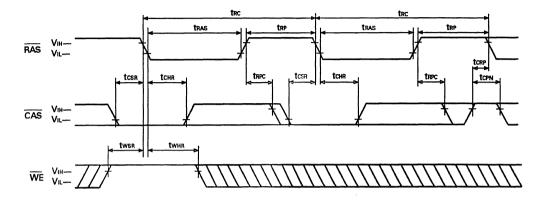
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode Read and Write Cycle



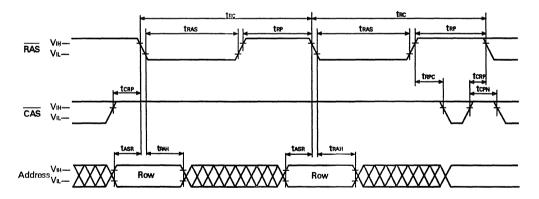
Romark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Refresh Cycle



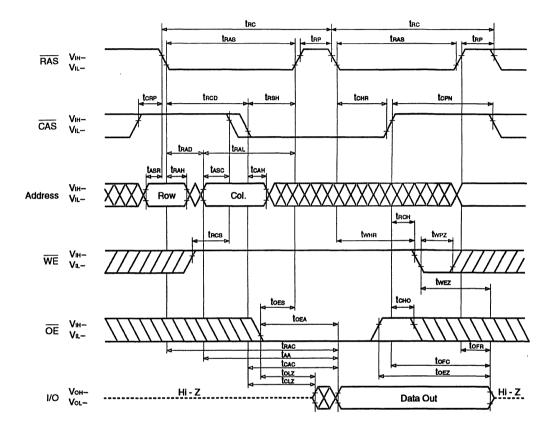
Remark 1. Address, OE : Don't care 2. I/O : Hi-Z

RAS Only Refresh Cycle

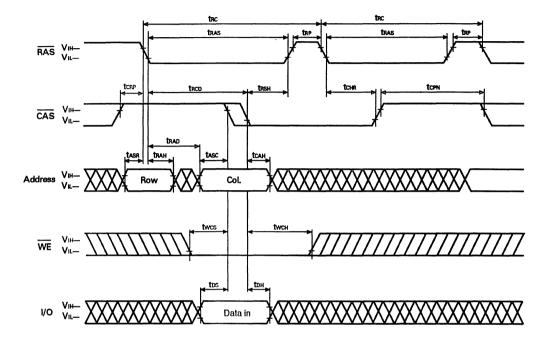


Remark 1. OE : Don't care 2. I/O : Hi-Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Remark OE: Don't care

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